الجمهوريـــة الجزائريـــة الديمقراطيـــة الشعبيـــة
The People's Democratic Republic of Algeria
وزارة التعليـــــــم   العالـــــي و البحـــث العلـــمي
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جامعة عمار ثليجي – الأغواط
University Amar Telidji of Laghouat

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Domain :…Science and Technology...
Field : … Electronic …
Speciality :…Microelectronic…

Course Handout (Lectures)
Intended for students of: . Master. Level: ... 1st year...

Design of MOS analog integrated circuits

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Foreword

This course material is part of the module: "*Design of MOS analog integrated circuits*", intended for first-year students, Academic Masters, option: "Microelectronics". This handout is developed with the aim of enabling the student to master the Design Flow of analog integrated circuit design.

This methodological module is credit 3, coefficient 2 with a weekly hourly volume of 03 hours at the rate of one course session and one supervised work session per week and a semester hourly volume of 37h30 hours.

This handout covers all the fundamental concepts of MOS analog integrated circuit design, starting with an introduction to the MOS transistor (some concepts of MOS capacitance and MOS structure are provided). The document is structured into three chapters, each developing a specific theme.

The first chapter: **The MOS transistor: deals with the NMOS and PMOS transistor with enhancement and depletion**: structure and operation, the model of the MOS transistor: linear model, quadratic model, operating regimes, the effect of substrate, electric field and channel modulation, and the Pspice model of the MOS transistor.

The second chapter: **Basic analog circuits using MOS technology:** focuses on current mirrors: analysis of different types of current mirrors, the offset circuit, the common source amplifier, differential amplification and the operational amplifier.

Finally, the third chapter, "**Mask Technology and Design**," covers the MOS technology manufacturing process, design rules, and mask design for a resistor, a MOS transistor, and an analog circuit.

Each chapter offers several exercises with fully detailed solutions.

Dr.Aissa Bellakhdar

Introduction to the MOS Transistor

Introduction

This introductory section lays the essential foundation of MOS technology. It presents the fundamental principles related to MOS capacitance, the structure of the component, and the operation of the NMOS transistor. It also introduces the different families of MOS transistors, giving readers a broad overview before delving into more technical aspects.

The MOS (Metal Oxide Semiconductor) transistor, or MOSFET (Metal Oxide Semiconductor Field Effect Transistors) is the most widely used semiconductor device at the base of every analog or digital circuit. It is present in high density in integrated circuits such as microprocessors or memories. It is therefore particularly important to understand the operation of: the MOS capacitor, the structure that is the basis of this MOS technology.

1- MOS Capacity

1-1 Structure

It consists of a metal-oxide-silicon stack.
A layer of insulating oxide (SiO_2) with a thickness of "x_{ox}" is sandwiched between a layer of metal (Al or highly doped silicon) and a silicon substrate.

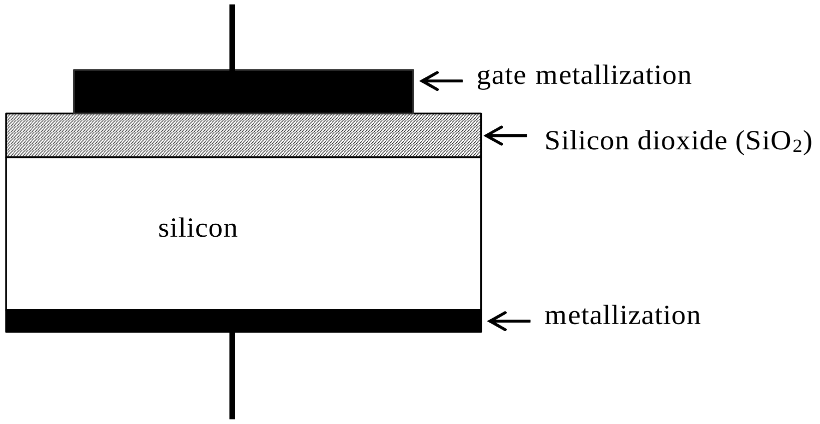
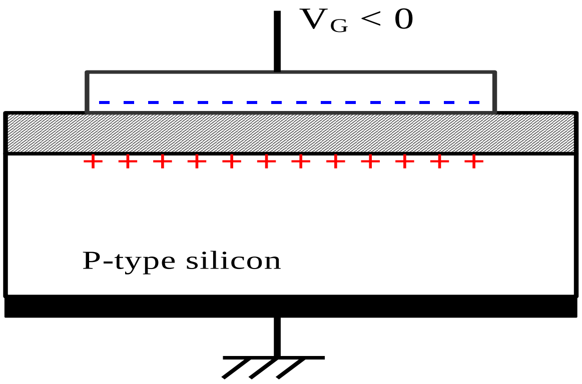


Fig.1

1-2 Operating regimes

Different regimes are defined depending on the polarization between these two electrodes.
Example of MOS capacitance on a P-type substrate.

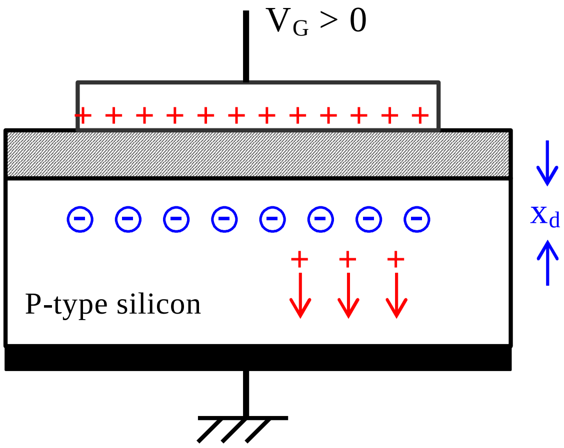
Accumulation regime



Accumulation of majority carriers on at the silicon surface

Fig.2

Depletion regime



Depletion regime

or

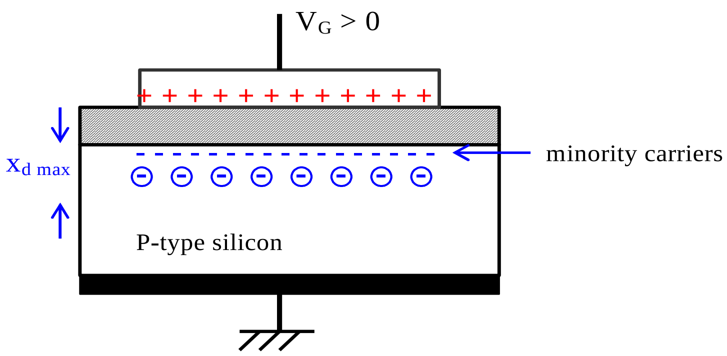
depletion at the silicon surface :

➔ The majority carriers are pushed back in depth

➔ The “fixed” negative ions remain

Fig.3

Inversion regime



An inversion layer is created on the surface of the silicon

➔ channel of the future MOS transistor

Fig.4

1-3 Electrical model of MOS capacitance and C(V) curve

The MOS capacitance is equivalent to two capacitances in series: the oxide capacitance (C_{ox}) and the semiconductor capacitance (C_{SC}).

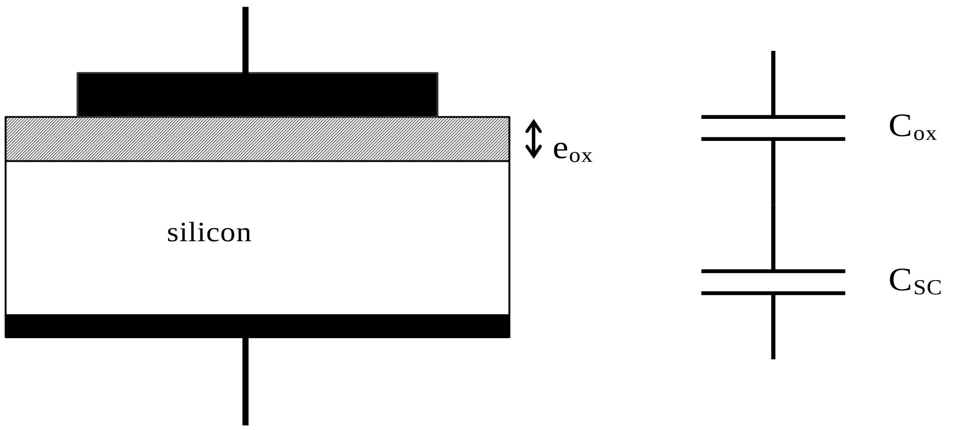


Fig.5

The total equivalent capacity (per unit area) is written as : $\frac{1}{C}=\frac{1}{C_{ox}}+\frac{1}{C_{SC}}$

With $C_{ox} = constant = \frac{\varepsilon_{ox}}{e_{ox}}$ $(\varepsilon_{r\_ox} \approx 3.9)$

$C_{SC}=\frac{\varepsilon_{SC}}{X_d}$ $(\varepsilon_{r\_SC} \approx 11.7)$

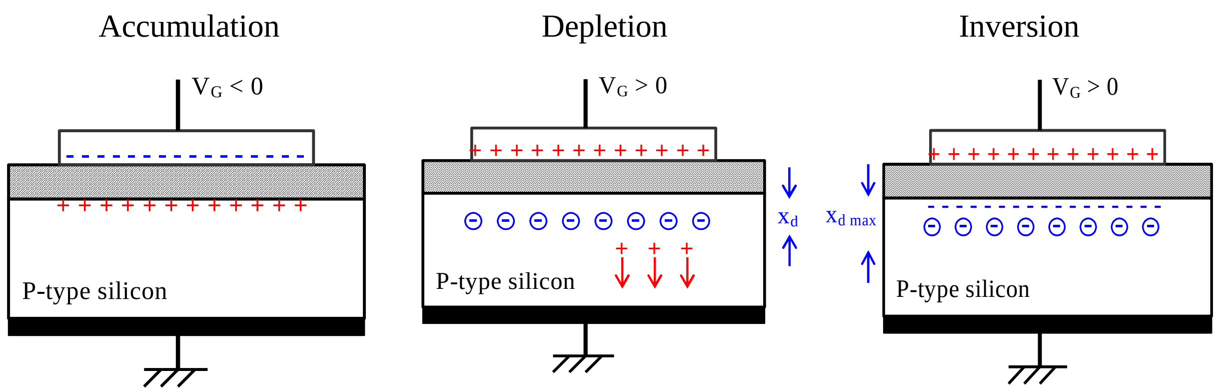


Fig.5

$C_{SC} >> C_{ox}$

$C \approx C_{ox} = C_{max}$

$\frac{1}{C}=\frac{1}{C_{ox}}+\frac{1}{C_{SC}}=f(V_G)$

$\frac{1}{C}=\frac{1}{C_{ox}}+\frac{1}{C_{SC,min}}=\frac{1}{C_{min}}$

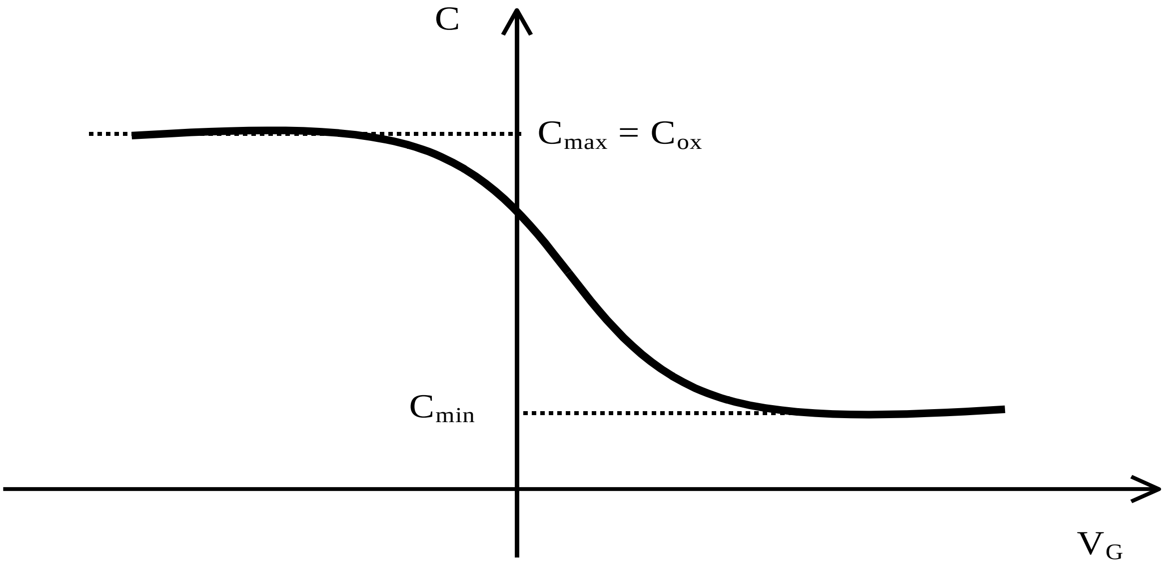


Fig.6

2- The MOS Structure

The N-channel MOS transistor (or MOSFET for **M**etal-**O**xide-**S**emiconductor **F**ield **E**ffect **T**ransistor) is a quadrupole device consisting of a gate electrode **(G),** source **(S),** drain **(D)** and substrate **(B).** The length of the transistor, denoted **L**, corresponds to the length of its gate and its width is denoted **W**. Conduction is ensured by the minority carriers of the substrate (electrons in the case of an NMOSFET), at the interface between the gate dielectric and the substrate.

As its name suggests, the operation of the field effect transistor (MOSFET) is based on the action of a vertical electric field. This field makes it possible to locally modulate the concentration of carriers in a semiconductor zone called the conduction channel or inversion channel, located between two charge reservoirs (the source and the drain). The electric field is governed by a control electrode, called the gate, through an insulating layer that constitutes the gate dielectric (Figure 7). There are two types of MOS (Metal Oxide Semiconductor) transistors:

- N-type or N-channel MOS transistors (NMOS) with P substrate
- P-type or P-channel MOS transistors (PMOS) with N substrate

An N-type transistor (NMOS) consists of:

- Substrate (silicon, Si) doped "p"
- Drain and source doped "n"
- Insulating layer (SiO2)
- Gate (aluminum or polysilicon).

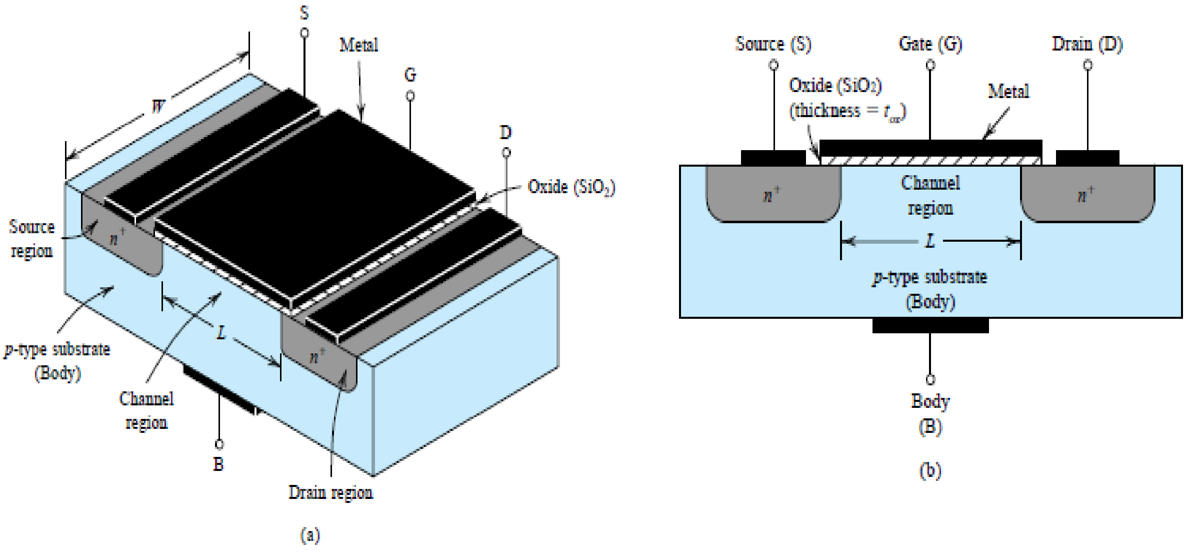
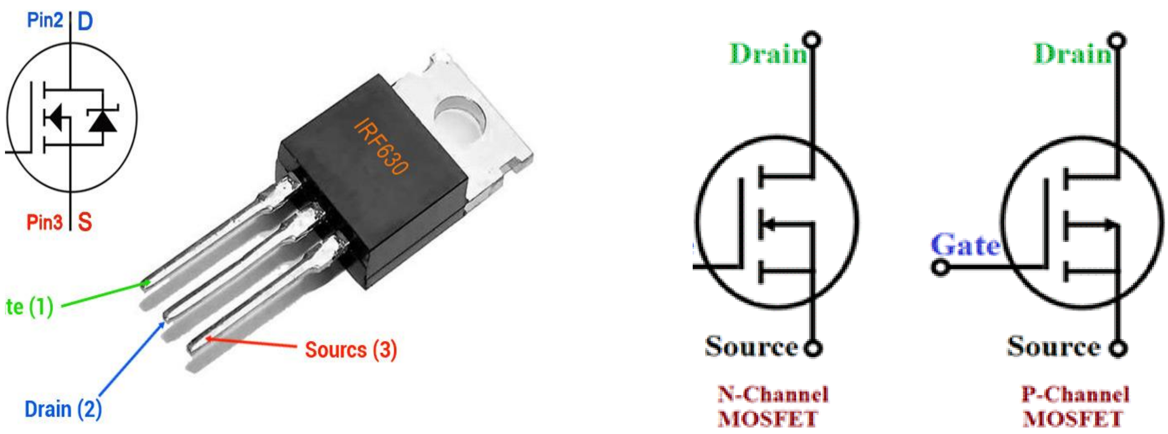


Fig.7 Physical structure of MOSFET, a) perspective view b) Cross sectional view



Electrical symbol of MOSFET

Fig.8 MOSFET: Metal Oxide Semiconductor Field Effect Transistor

In an N-doped zone, the majority charge carriers are electrons (they are holes in the case of a .P-type zone). For a P-type transistor, the dopings are reversed.

3- How NMOS Transistor Works ?

Let's apply an electric field $\vec{E}$ between grid and source, we can have 3 operating regimes

- Accumulation Regime
- Depletion Regime
- Inversion Regime

3.1- Accumulation Regime

If Vgs < 0, the electric field $\vec{E}$ attracts the holes on the surface of the SC (oxide/SC interface), there is accumulation of positive charges, so that electrical neutrality is maintained. Therefore, electrons appear under the gate.

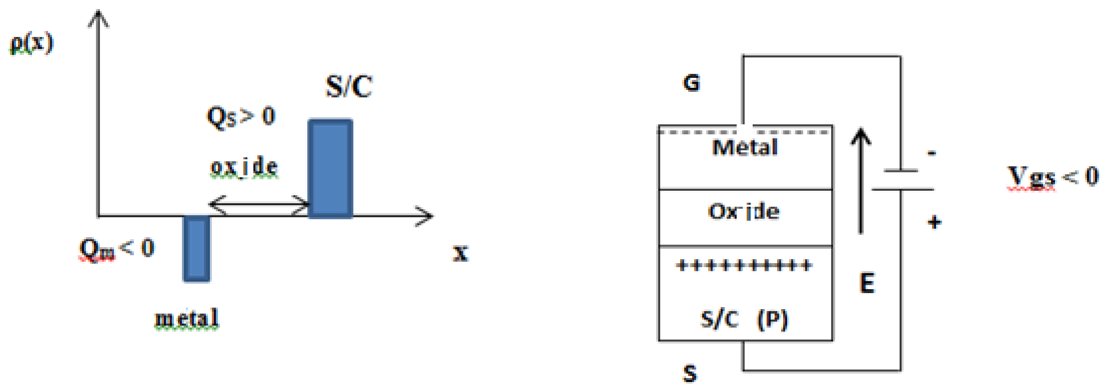


Fig.9 Polarization and charge density in a MOS structure (Accumulation Regime)

3.2- Depletion Regime

If Vgs > 0, and Vgs < VT (threshold voltage), the electric field $\vec{E}$ repels the holes on the surface, there will be creation of a space charge zone (SCZ) empty of free carriers and negatively charged by fixed ions, because the acceptor atoms are no longer neutralized by the holes. There is therefore the appearance of positive charges to satisfy electrical neutrality.

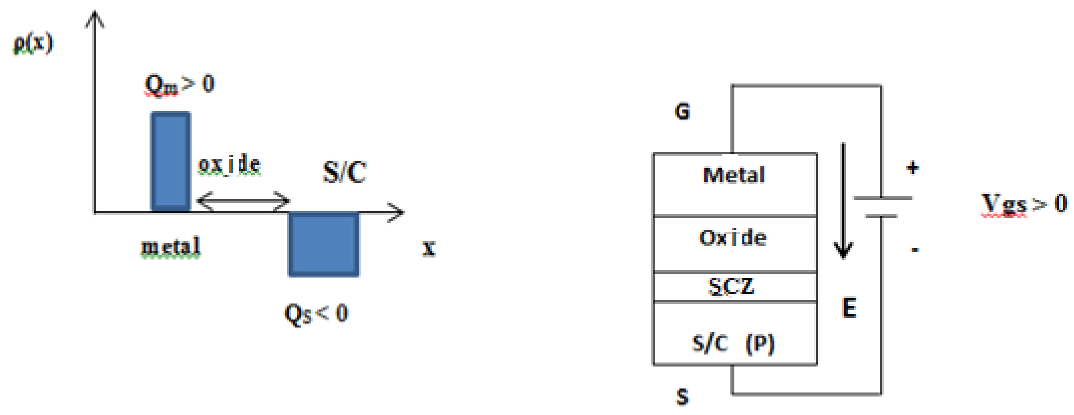


Fig.10 Polarization and charge density in a MOS structure (Depletion Regime)

3.3- Inversion Regime

If Vgs > 0, and Vgs > VT (inversion threshold voltage), the resulting low intensity electric field $\vec{E}$:

- Repels the majority carriers (holes in our case) in the bulk, creating a space charge zone (SCZ)

- But it also attracts the minority electrons at the surface. Thus, an N-type channel (inversion channel) is created.

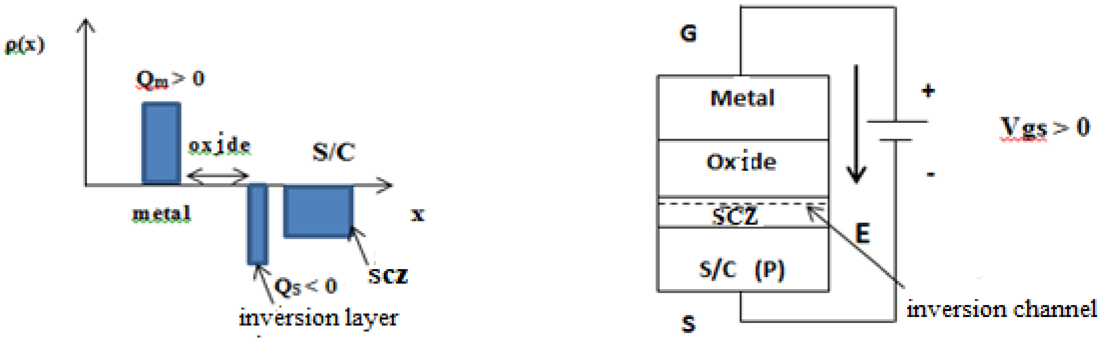


Fig.11 Polarization and charge density in a MOS structure (Inversion Regime)

4- Different Types of Transistors

Depending on the type of semiconductor constituting the Substrate, we can distinguish two types of transistors; NMOS transistors or N-channel transistors designed on a p-type substrate and PMOS transistors or P-channel MOS transistors designed on an n-type substrate.

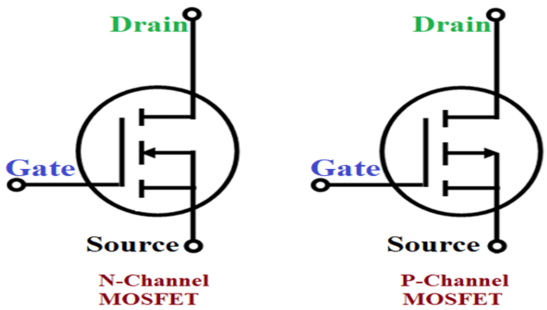
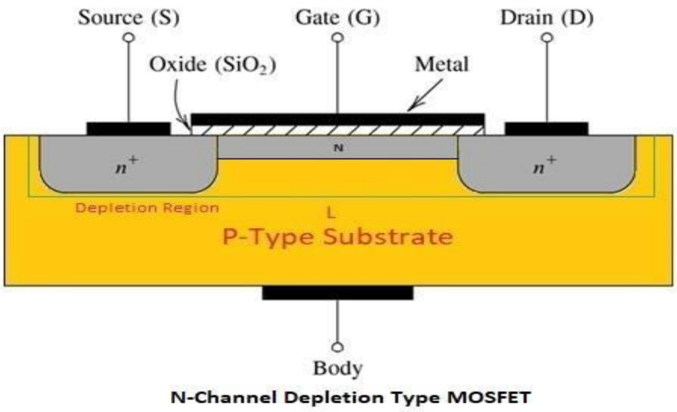
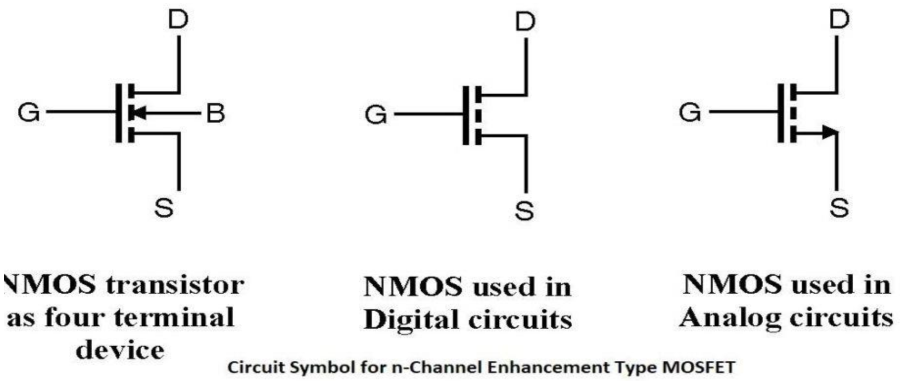


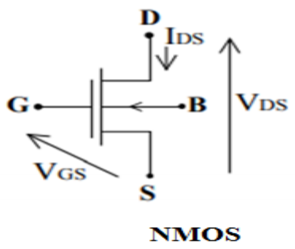
Fig.12 NMOS and PMOS Structure

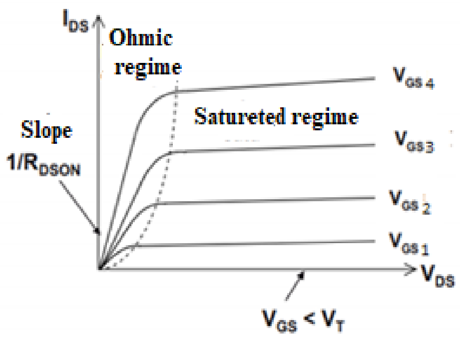
4.1 N-channel MOS transistor (NMOS) ($V_{DS} \geq 0$)

In the case of N-channel NMOS transistors, the gate is biased by a positive voltage V_{GB}, in order to create a depletion zone populated by electrons at the SC/Insulator interface. The source and drain are connected by a channel formed by electrons. The potential difference between the drain and the source, called V_{DS}, is positive, the direction of the current is from the source to the drain.









Circuit symbol

I-V characteristics of NMOS Transistor

Fig.13 : N-channel MOS transistor

Transistor NMOS conduction equations

- **Blocked regime:**

$V_{GS} < V_{TN}$ (electric insulation between drain and source)

- **Saturated regime:**

$V_{GS} > V_{TN}$

- If $V_{DS} < (V_{GS}-V_{TN})$ ohmic regime

$$I_{DS} = \beta_N \left((V_{GS} - V_{TN}) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

- If $V_{DS} > (V_{GS}-V_{TN})$ saturated regime, V_{TN} : threshold voltage

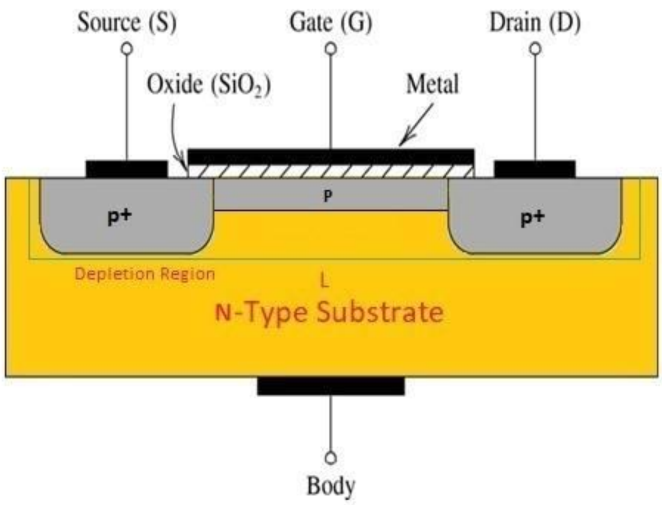
$$I_{DS} = \frac{\beta_N}{2} (V_{GS} - V_{TN})^2$$

$$\beta_N = \mu_{ns} C_{ox} \frac{W}{L}$$

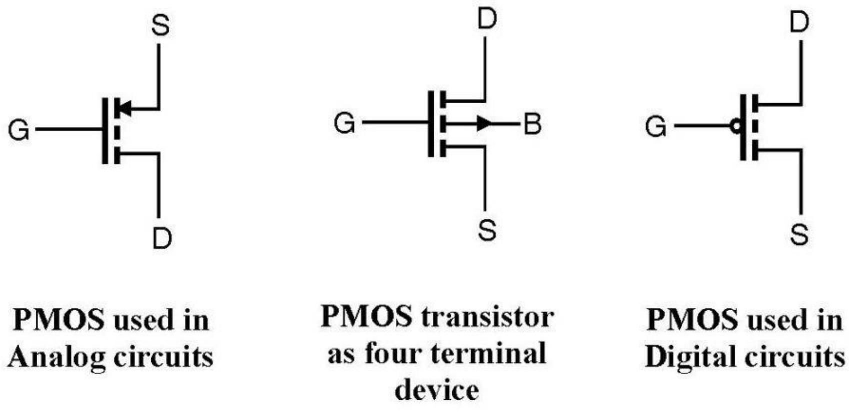
$$R_{DSON} = \frac{1}{\beta_N (V_{GS} - V_{TN})}$$

4.2 P-Channel MOS Transistor (PMOS) ($V_{DS} \leq 0$)

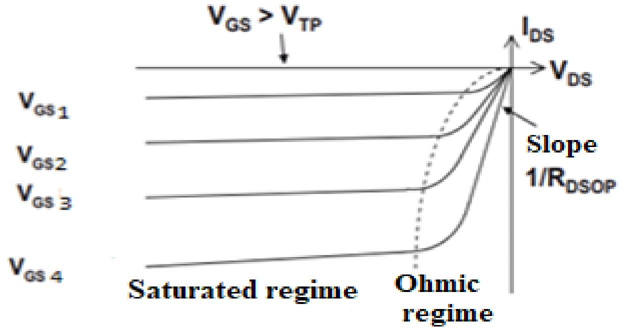
For P-channel PMOS transistors, the gate is negatively biased, the depletion zone at the SC/Insulator interface is populated by holes, the conduction channel is formed by holes, and the V_{DS} voltage must be negative to drain these holes. The current flows in the same direction as the hole movement, i.e. from source to drain**.**

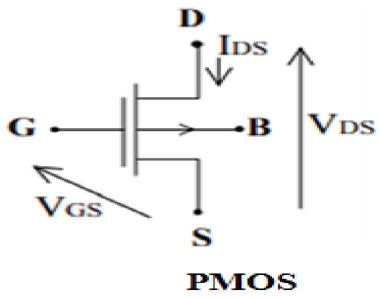


P-channel Depletion Type MOSFET



Circuit symbol for p-channel EMOSFET





Circuit symbol I-V characteristics of PMOS Transistor

Fig.13 : P-channel MOS transistor

PMOS transistor conduction equations

- **Blocked regime:**

$V_{GS} > V_{TP}$ (electric insulation between drain and source)

- **Saturated regime:**

$V_{GS} < V_{TP}$

- If $V_{DS} > (V_{GS}-V_{TP})$ ohmic regime

$$I_{DS} = -\beta_P \left((V_{GS} - V_{TP})V_{DS} - \frac{V_{DS}^2}{2} \right)$$

- If $V_{DS} < (V_{GS}-V_{TP})$ saturated regime, V_{TP} : threshold voltage

$$I_{DS} = -\frac{\beta_P}{2}(V_{GS} - V_{TP})^2$$

$$\beta_P = \mu_{ps} C_{ox} \frac{W}{L}$$

$$R_{DSOP} = -\frac{1}{\beta_P (V_{GS} - V_{TP})}$$

$$\mu_{ns} \approx 3\mu_{ps}$$

Summary :

1- Structure :

The MOS transistor changes state depending on the gate voltage Vg (control voltage) relative .to the threshold voltage V_T (technological constant).

- $Vg < V_T$ ⟶ blocking case: the source and the drain are isolated by the PN junctions (diodes).

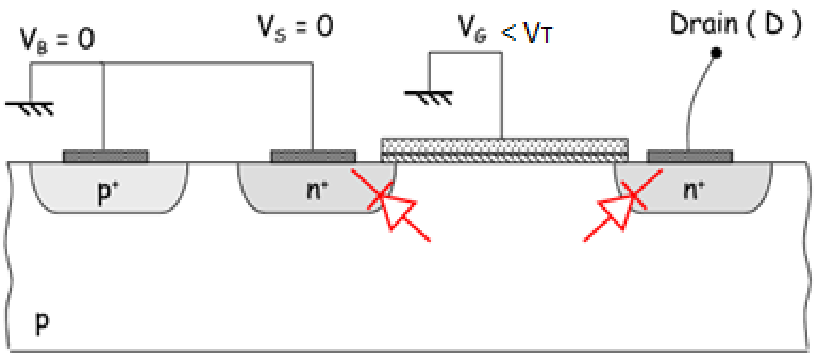


Fig.14 Blocking Transistor

- $Vg > V_T$ ⟶ passing case: free electrons from the substrate (minority carriers) are attracted under the gate ⟶ polarity inversion ⟶ flow of current I_D in the N-type layer between the drain and the source.

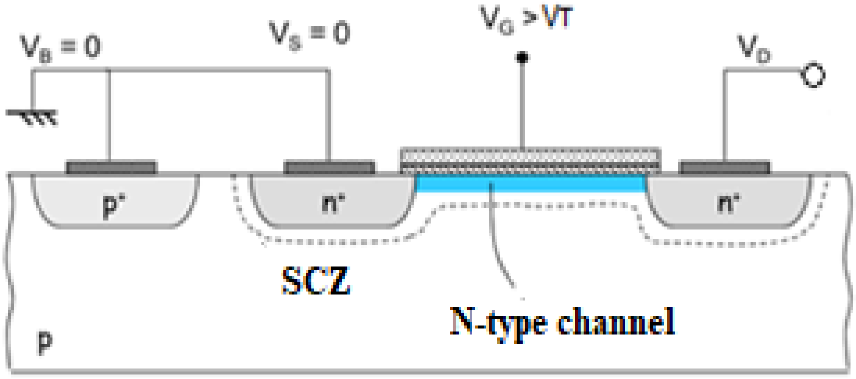


Fig.15 Passing Transistor

Conclusion :

This introductory section lays the essential foundation of MOS technology. It presents the fundamental principles related to MOS capacitance, the structure of the component, and the operation of the NMOS transistor. It also introduces the different families of MOS transistors, giving readers a broad overview before delving into more technical aspects.

Chapter I: The MOS transistor

Introduction

This chapter explores in detail the structure, operation, and modeling of the MOS transistor, focusing on NMOS and PMOS in both enhancement and depletion modes. It also provides a clear classification of the different operating regions (saturation, linear, cut-off), while addressing significant secondary effects such as the substrate effect and channel length modulation. The SPICE model is explained with a complete methodology to simulate the transistor behavior, making this section fundamental for any circuit designer.

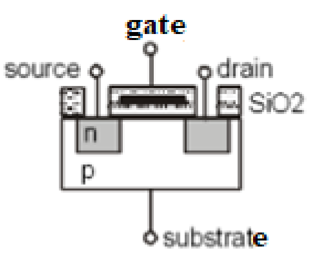
The two basic types of MOSFETs are depletion MOSFETs (D-MOSFETs) and enhancement MOSFETs (E-MOSFETs). Within each type of MOSFET, we can distinguish between N-channel MOSFETs (current comes from the movement of electrons) and P-channel MOSFETs (current comes from the movement of holes).

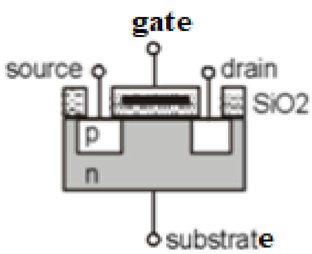
There are two types of MOSFET field-effect transistors:

- ✓ N-channel MOSFET (enhancement- or depletion-mode)
- ✓ P-channel MOSFET (enhancement- or depletion-mode).

I.1 The NMOS and PMOS enhancement-mode transistor: structure and operation

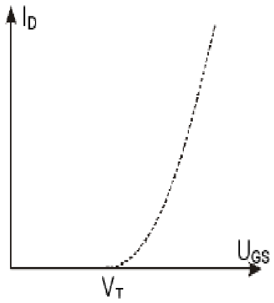
The enhancement-mode MOS (Metal Oxide Semiconductor) transistor is a field-effect transistor. It consists of two doped regions of identical polarity integrated into a region of reverse polarity. The space between these two regions defines the MOS channel. A gate exactly overlaps the channel. This gate is insulated from the channel by a thin layer of silicon oxide (SiO2). An electrode is connected to each end of the channel. A third electrode is connected to the gate. The substrate that serves as the physical support for the element is connected to a fourth electrode. This electrode is most often connected to the source electrode. As with JFETs, two structures are possible: n-channel and p-channel enhancement-mode MOS.





a) Structure of n-channel MOS transistor Fig I.1 b) Structure of p-channel MOS transistor

- **Voltage-current relationship:**



• The drain-to-source current is controlled by the gate-to-source voltage.

• The gate-to-source voltage can be negative or positive.

• If the gate-to-source voltage falls below a certain value,

V_T (called the threshold voltage), the drain-to-source current is interrupted

• A gate-to-source voltage greater than VT increases the drain-to-source current.

b- Electrical symbol :

c) n-channel MOS transistor d) p-channel MOS transistor

c- Production and technology

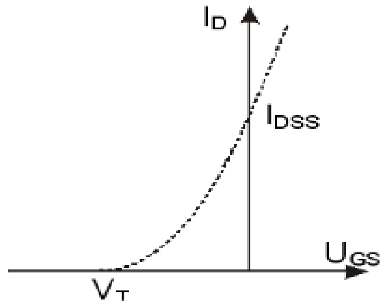
Like diodes, these elements are most often made of silicon. They are used to make amplifiers, but especially to make the digital circuits that make up most of today's electronic devices. They are also frequently used for power control (motors, lamps, etc.).

I.2 The NMOS and PMOS depletion transistor: structure and operation

The MOS (Metal Oxide Semiconductor) depletion transistor is a field-effect transistor. It consists of a doped semiconductor channel and a gate that exactly overlaps the channel. This gate is insulated from the channel by a thin layer of silicon oxide (SiO2). An electrode is connected to each end of the channel. A third electrode is connected to the gate. The substrate that serves as the physical support for the element is connected to a fourth electrode. This electrode is most often connected to the source electrode. As with JFETs, two structures are possible: n-channel and p-channel depletion MOS.

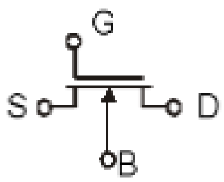
a) Structure of n-channel MOS transistor Fig.I.2 b) Structure of p-channel MOS transistor

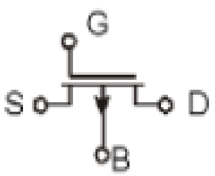
- **Voltage-current relationship:**



- The drain-to-source current is controlled by the gate-to-source voltage.
- The gate-to-source voltage can be negative or positive.
- A negative gate-to-source voltage decreases the drain-to-source current.
- A positive gate-to-source voltage increases the drain-to-source current.
- If the gate-to-source voltage exceeds a certain value V_T (called the threshold voltage), the drain-to-source current is interrupted.

b- Electrical symbol :





c) n-channel MOS transistor d) p-channel MOS transistor

c- Production and technology

Like diodes, these elements are most often made of silicon. They are used to make amplifiers.

Note: The most commonly used transistor is the enhancement-mode MOSFET (N-channel).

Conduction conditions

The conductive channel exists if the gate voltage is higher (case of the NMOS transistor) or lower (case of the PMOS transistor) than a threshold voltage Vth, and this is for an enhancement transistor (Table I.1)

Tableau I.1 : MOSFET conduction condition

Channel	Type	Carriers	Conduction condition
N	Enhancement	Electrons	Vgs > Vth
N	Depletion	Electrons	Vgs < Vgsoff
P	Enhancement	Holes	Vgs < Vth
P	Depletion	Holes	Vgs > Vgsoff

Below is a table resulting from the different types of transistors with their output and transfer characteristics (Table I.2).

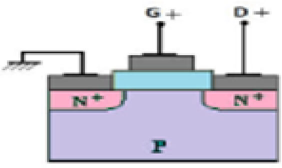
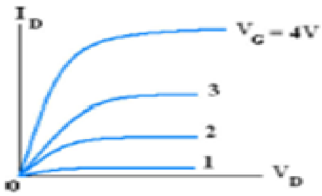
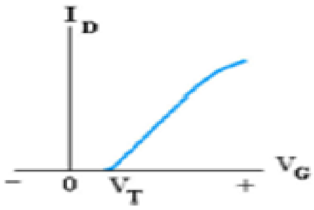
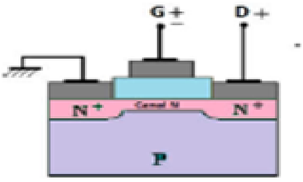
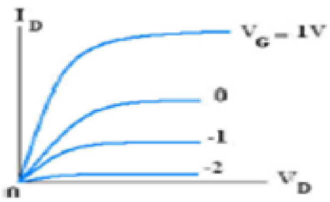
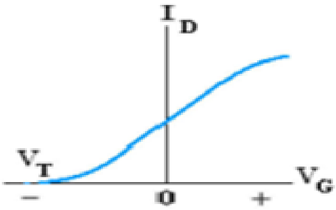
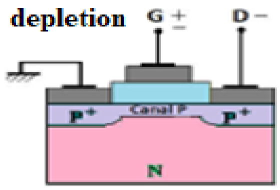
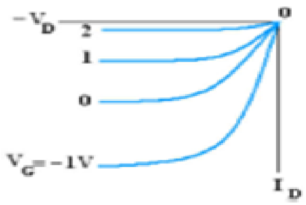
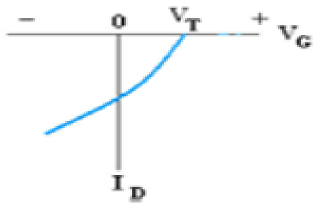
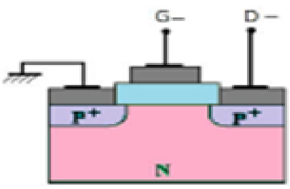
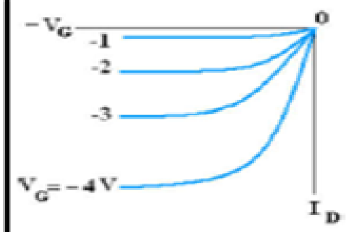
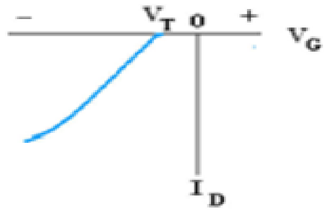
Types	*Output characteristics*	*Transfert characteristics*
NMOSFET (normally off) **enhancement** 		
NMOSFET (normally on) **depletion** 		
PMOSFET (normally on) **depletion** 		
PMOSFET (normally off) 		

Table I.2: Output and transfer characteristics of different types of MOSFETs

I.3 MOS transistor model: linear model, quadratic model

I-3-1 Calculation of the current flowing in the channel of a MOSFET

The conductance of an infinitesimal channel element of length dx, width W and thickness dy, at point M(x,y) (see figure I.1) is written :

$$W.q.\mu.n(x,y).\frac{dy}{dx} \tag{I.1}$$

By integrating this equation from 0 to $y_1(x)$ (see figure), we obtain the conductance of the slice of length dx and thickness $y_1(x)$:

$$dG = q \cdot \frac{W \cdot \mu_n}{dx} \cdot \int_0^{y_1} n(x,y) \cdot dy \qquad \text{(I.2)}$$

Donc la résistance d'un élément du canal d'épaisseur dx comprise entre x et x+dx est :

$$dR = -\frac{dx}{W \cdot \mu_n \cdot Q_I(x)} \qquad \text{(I.3)}$$

When :

$$Q_I(x) = -q \cdot \int_0^{y_l} n(x,y) \qquad \text{(I.4)}$$

represents the charge at the abscissa x of the inversion layer. It can be expressed as :

$$Q_I(x) = -C_{ox} \cdot (V_{GS} - V_T - V(x)) \qquad \text{(I.5)}$$

C_{ox} being the capacitance of the oxide layer per unit area .

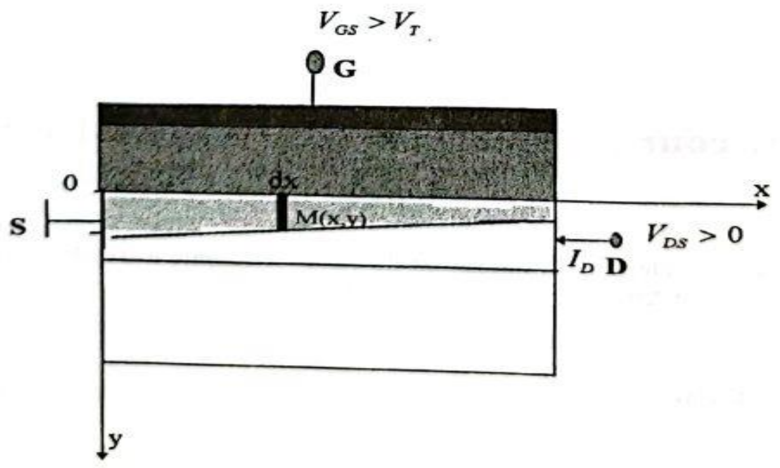


Fig I.2 MOS transistor model

The infinitesimal element dx being assumed to be equipotential, Ohm's law applied to the terminals of this element is written :

$$I_D = \frac{dV}{dR} \qquad \text{(I.6)}$$

Replacing *dR* with its expression given by the equation (I.3), we obtain :

$$I_D = W \cdot \mu_n \cdot C_{ox} \cdot (V_{GS} - V(x) - V_T) \cdot \frac{dV(x)}{dx} \qquad \text{(I.7)}$$

This equation can be put in the form :

$$I_D \cdot dx = W \cdot \mu_n \cdot C_{ox} \cdot (V_{GS} - V(x) - V_T) \cdot dV(x) \qquad \text{(I.8)}$$

The integration of the 2 members of this equation between x = 0 (V(0) = 0) and x = L (V(L) = V_{DS}) given :

$$\int_0^L I_D \cdot dx = \int_0^{V_{Ds}} W \cdot \mu_n \cdot C_{ax} \cdot (V_{GS} - V(x) - V_T) \cdot dV(x) \qquad \text{(I.9)}$$

Which gives : $$I_D = \mu_{n.} C_{ox}.\frac{W}{L}\left[(V_{GS} - V_T).V_{DS} - \frac{V_{DS}^2}{2}\right] \quad (I.10)$$

We put : $$K_n = \mu_{n.} C_{ox}.\frac{W}{2L} \quad (I.11)$$

The current can then be put in the form :

$$I_D = K_n[2(V_{GS} - V_T).V_{DS} - V_{DS}^2] \quad (I.12)$$

We will consider two operating cases: the unpinched regime and the pinched or saturated regime.

- **Unpinched regime : $V_{DS} < V_{GS} - V_T$**

In this case, the inversion layer exists at every point in the channel.

- For very low drain voltages such as :

$$V_{DS} \ll (V_{GS} - V_T) \text{ then } V_{DS}^2 \ll (V_{GS} - V_T).V_{DS} \quad (I.13)$$

The inversion layer is practically homogeneous (see figure), in this case we are in the ohmic regime, and the expression can be put in the form :

$$I_D = 2K_n(V_{GS} - V_T).V_{DS} \quad (I.14)$$

The current in this case varies linearly with the voltage applied to the drain .

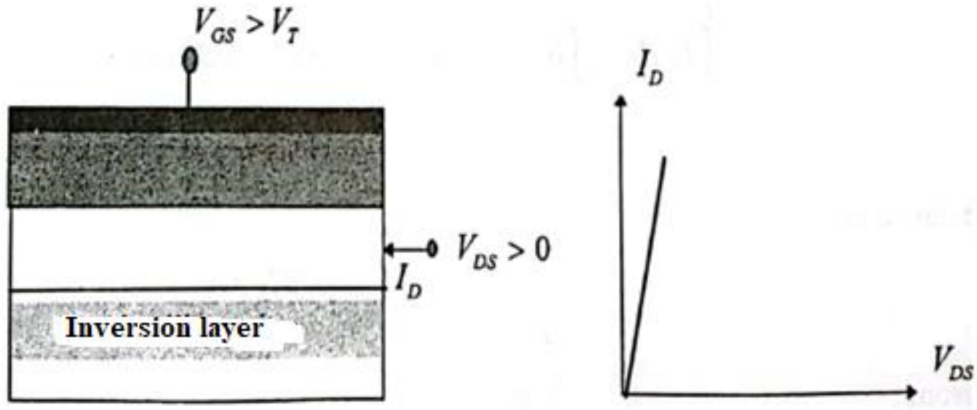


Fig I.3 MOS transistor model, unpinched regime

- For low or medium drain voltages, the inversion layer is no longer uniform (see figure ..), the drain current increases less quickly than the drain-source voltage because the term $\left(\frac{V_{DS}^2}{2}\right)$ is no longer negligible in the expression of the current and we have :

$$I_D = K_n.[2(V_{GS} - V_T) - V_{DS}].V_{DS} \quad (I.15)$$

For ($V_{DS} = V_{GS} - V_T = V_{DSsat}$) the inversion layer disappears at the end of the drain. We enter the pinched or saturated regime.

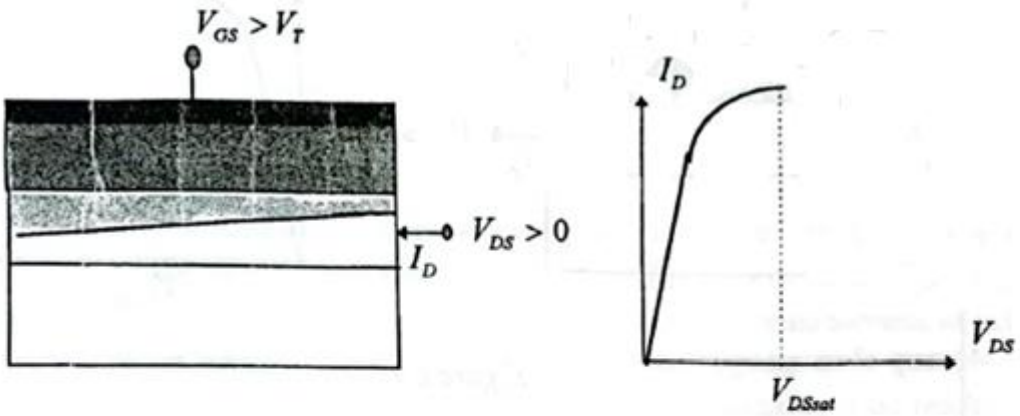


Fig I.4 MOS transistor model, pinched regime

- **Pinched or saturated regime :** $V_{DS} \geq V_{GS} - V_T$

The saturation therefore begins for the drain-source voltage $V_{Dssat} = V_{GS} - V_T$. Le courant de drain peut alors être mis sous la forme :

$$I_D = K_n.(V_{GS} - V_T)^2 \quad \text{(I.16)}$$

or even :

$$I_D = K_n.V_{DSsat}^2 \quad \text{(I.17)}$$

In this case the channel pinches at the drain as shown in the figure …

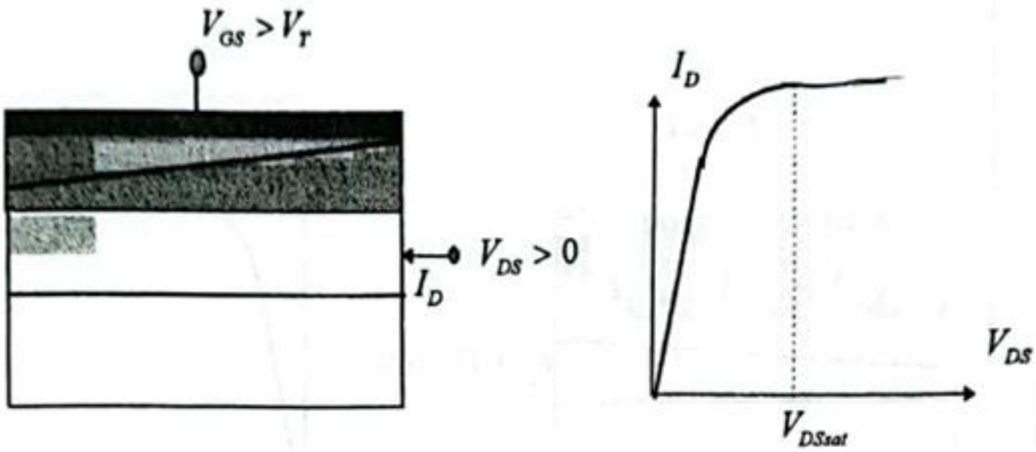


Fig I.5 MOS transistor model, saturated regime

Table III.2 provides information on the design rules used by MICROWIND.

- **Modèle petits signaux simplifié**

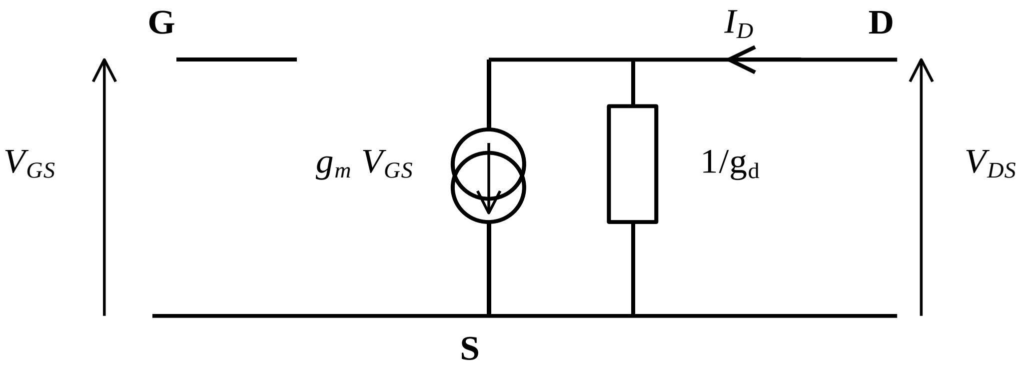


Fig.I.6

g_m: transconductance $\qquad g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}=cste}$

g_d: conductance du canal $\qquad g_d = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_G=cste}$

Régime ohmique (linéaire)

$$g_d = \mu \frac{W}{L} C_{ox} V_{DS}$$

Régime de saturation

car $\lambda \cdot V_{DS} << 1$

$$g_m = \mu \frac{W}{L} C_{ox}(V_{GS} - V_T)$$

$$g_m = \sqrt{\mu \frac{2W}{L} C_{ox}} \sqrt{I_D}$$

(I.18)

I-3-2 Current-voltage characteristics in the ideal case

From the expressions for drain current as a function of drain-source voltage, we can plot the output characteristics of the MOSFET, which are given in Fig I.7 We have limited the unsaturated region to the region to the left of the dotted curve, and the saturated region to the right.

In the ideal case, and after saturation, the I_D (V_{DS}) characteristics are horizontal.

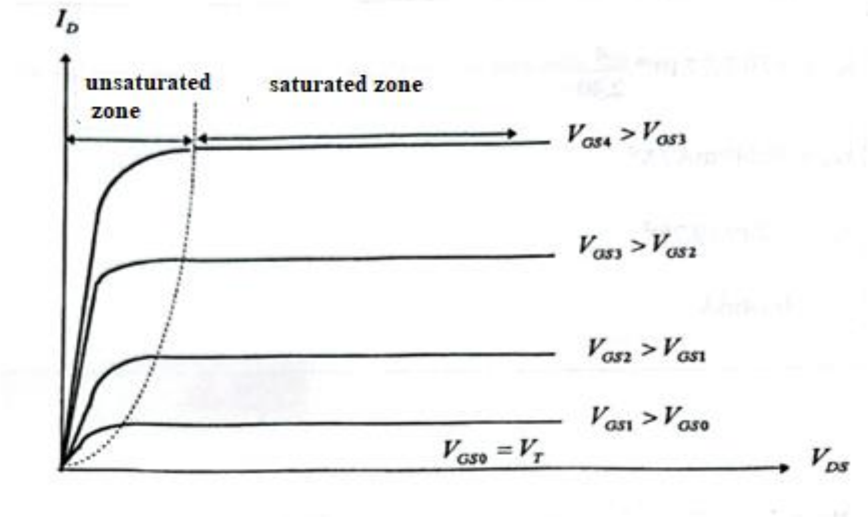


Fig I.7 $I_D(V_{DS})$ characteristics in the ideal case

In saturation mode and based on the expression (I.16) we can draw the $I_D(V_{DS})$ transfer characteristic given in Fig I.8.

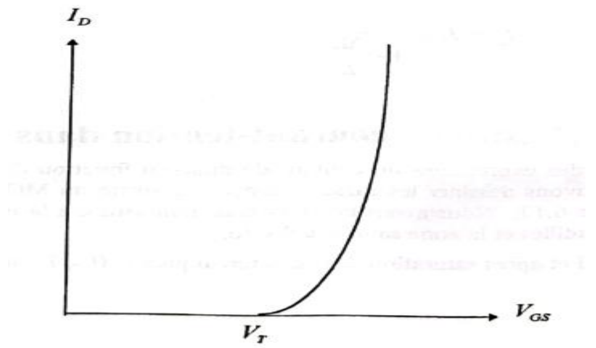


Fig I.8 transfer characteristic

I-3-3 Characteristic parameters of a MOSFET

I-3-3-1 Transconductance

Transconductance is defined by :

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS=cte}} \qquad \text{(I.19)}$$

- In unpinched regime :

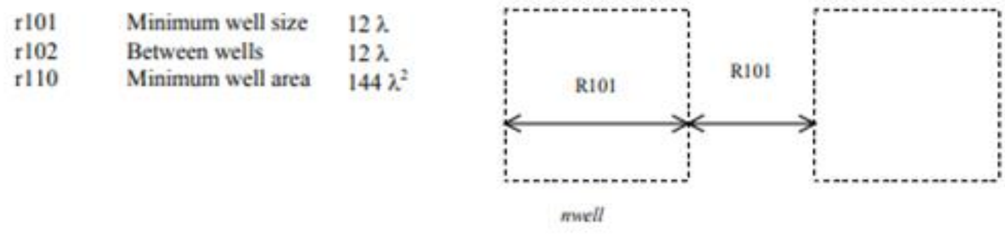
$$g_m = \left(\mu_n . C_{ox} . \frac{W}{L}\right) . V_{DS} \qquad \text{(I.20)}$$

Table III.2 Design rules used by MICROWIND

g_m is independent of V_{GS} but varies linearly with V_{DS} .

N-Well

- In a pinc

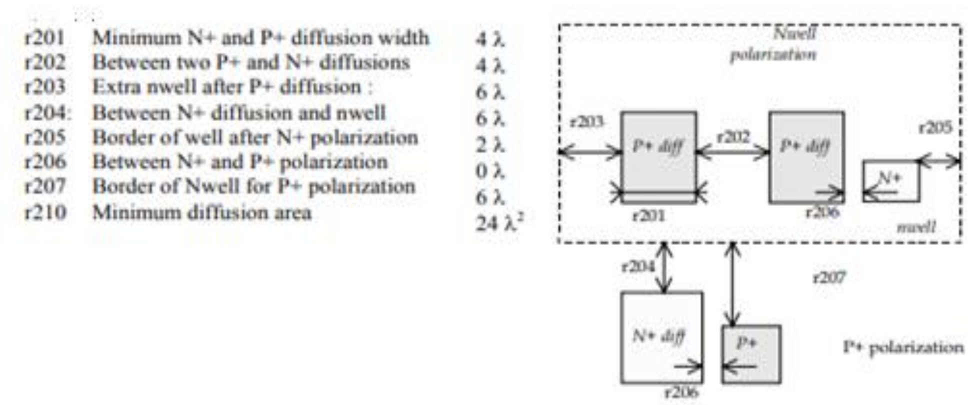


g_m varies linearl

I-3-3-2 Output

Diffusion

The conductan



In pinched reg
should be zero

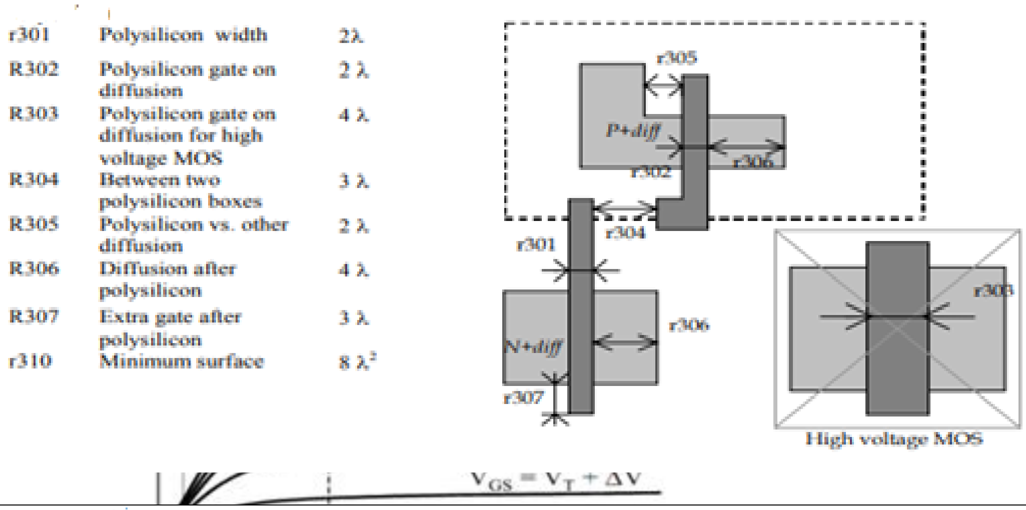
The existence
paragraph (I.3.

I. 4 MOSFET operating regimes

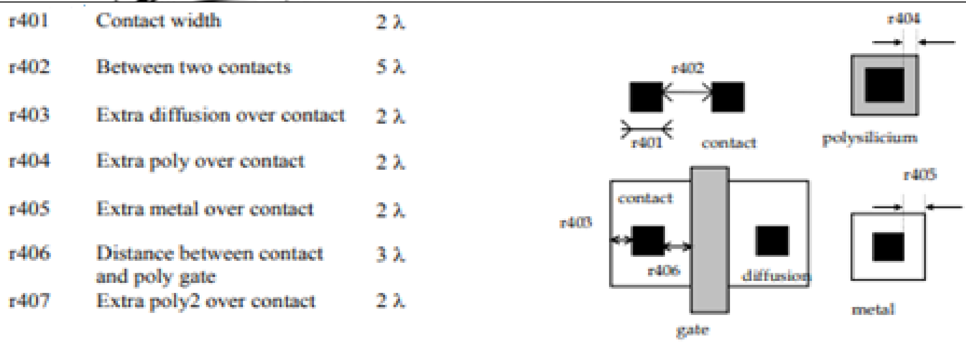
Polysilicon

Depending on t

regimes: linear



Contact



Applying an el
1.10 shows an
weak inversion regime.

• Minimum width of PolySi and diffusion line 2λ

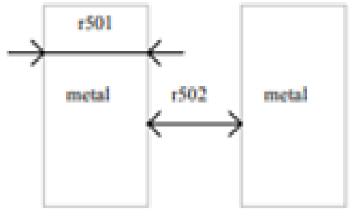
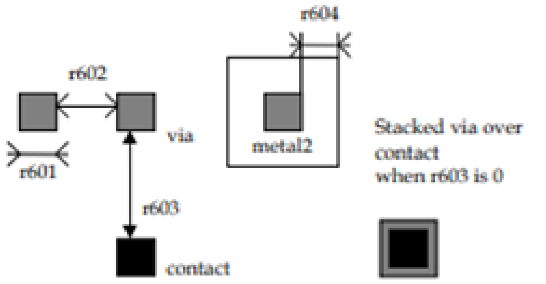
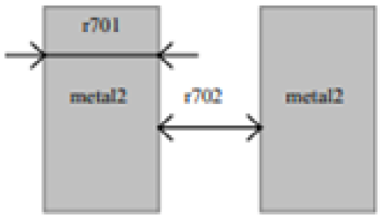
Metal 1	r501	Metal width	4 λ	
	r502	Between two metals	4 λ	
	r510	Minimum surface	16 λ^2	
Via	r601	Via width	2 λ	
	r602	Between two Via	5 λ	
	r603	Between Via and contact	0 λ	
	r604	Extra metal over via	2 λ	
	r605	Extra metal2 over via:	2 λ	
Metal 2	r701	Metal width::	4 λ	
	r702	Between two metal2	4 λ	
	r710	Minimum surface	16 λ^2	

Fig I.10. Band diagram of an N-MOSFET transistor (a) in flat band regime and in (b) weak inversion regime.

Let χ_{Si} be the ... of the conduct... the work functions of the metal and the semiconductor, Φ_f is the Fermi potential. Ψ_s is the potential difference between the surface and the bulk (the surface potential).

The Fermi level is given by : $$E_F = E_i - q\phi_f \qquad (I.23)$$

The Fermi level Φ_f is given by the following equation in the case of moderate doping :

$$\phi_f = \frac{kT}{q} ln\frac{N_A}{n_i} \qquad (I.24)$$

k is the Boltzmann constant, T is the temperature , q is the elementary charge and n_i is the intrinsic concentration of carriers in the material.

I.4.1 Triode regime

a- I_D -V_{DS} characteristics

For $V_{GS} \geq Vtn$ and $V_{DS} \leq V_{GS} - Vtn$:

• Minimum width of **metal line 3λ** because metal lines extend over a more uneven surface than other conductive layers to ensure continuity.

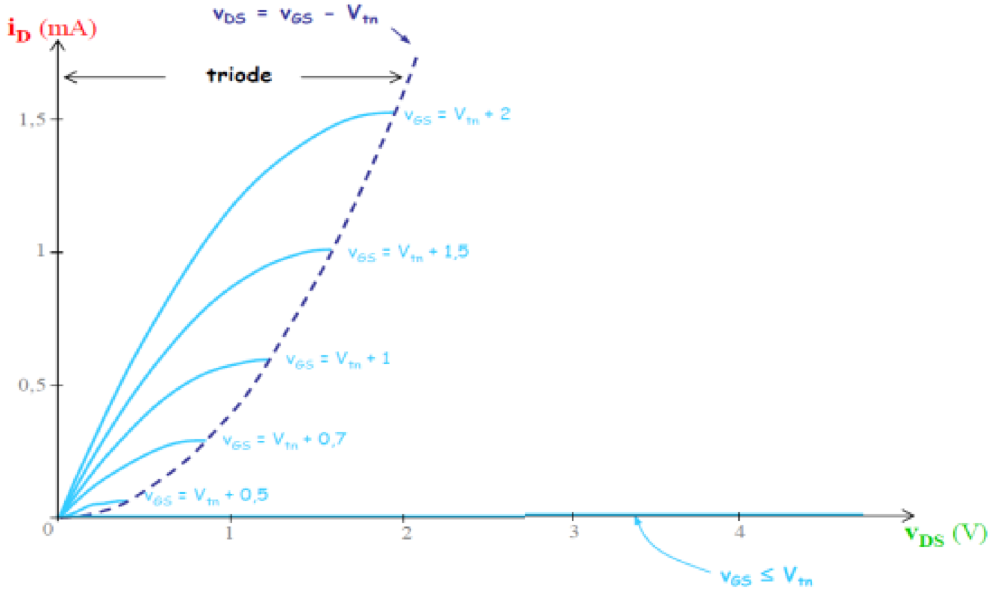


Fig I.11. I_D -V_{DS} Characteristics in triode regime

$$I_D = k' \frac{W}{L}\left[(V_{GS} - V_{tn})V_{DS} - \frac{V_{DS}^2}{2}\right] \quad (I.25)$$

With $$k'_n = \mu_n C_{ox} \quad (I.26)$$

K'_n NMOS gain factor [μA/V²]

μ_n electron mobility [cm²/Vs]

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \quad (I.27)$$

C_{ox} : Gate surface capacity [F/cm²]

t_{ox} gate oxide thickness [nm]

ε_{ox} permittivity of SiO2 [F/m]

b- Linear zone

For $V_{DS} << 2(V_{GS} - Vtn)$

$$I_D = k' \frac{W}{L}(V_{GS} - V_{tn})V_{DS} \quad (I.28)$$

$$r_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{1}{k' \frac{W}{L}(V_{GS} - V_{tn})}$$

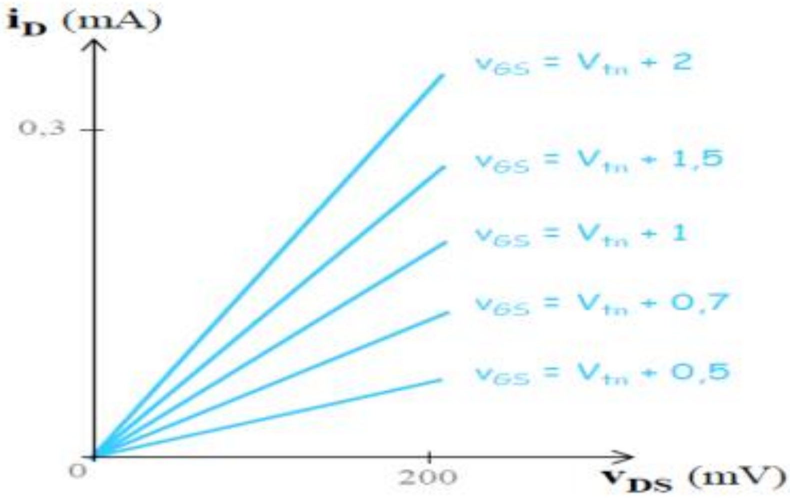


Fig I.12. I_D -V_{DS} characteristics in linear zone

I.4.2 Satureted regime

a- I_D – V_{DS} charactéristics

For $V_{GS} \geq Vtn$ and $V_{DS} \geq V_{GS} - Vtn$:

$$I_D = \frac{1}{2} k' \frac{W}{L} (V_{GS} - V_{tn})^2 \qquad (I.29)$$

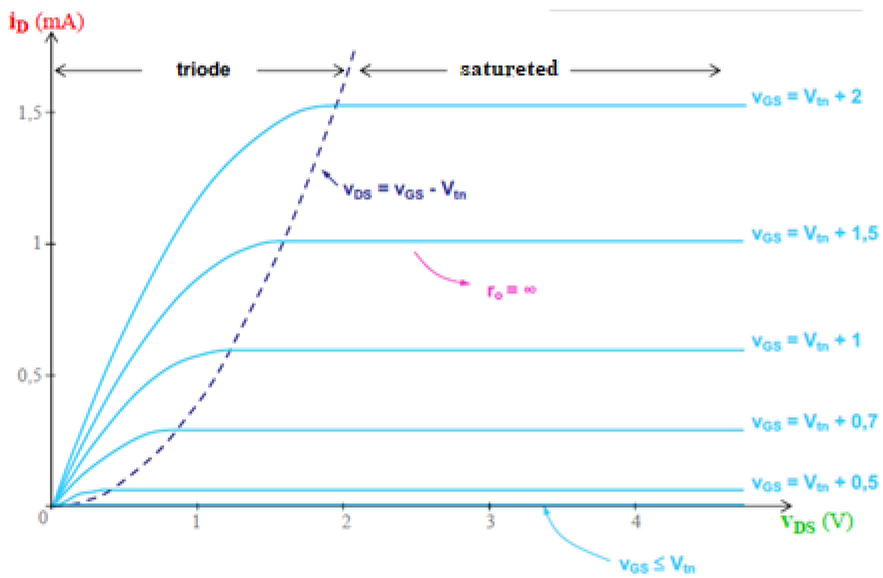


Fig I.13. I_D – V_{DS} characteristics in satureted regime.

b- I_D – V_{GS} caractéristics

For $V_{GS} \geq Vtn$ and $V_{DS} \geq V_{GS} - Vtn$:

The transconductance has a constant drain voltage V_{DS}, it is given by :

$$g_m = \frac{I_{DS}}{V_{DS}} \quad \text{(I.30)}$$

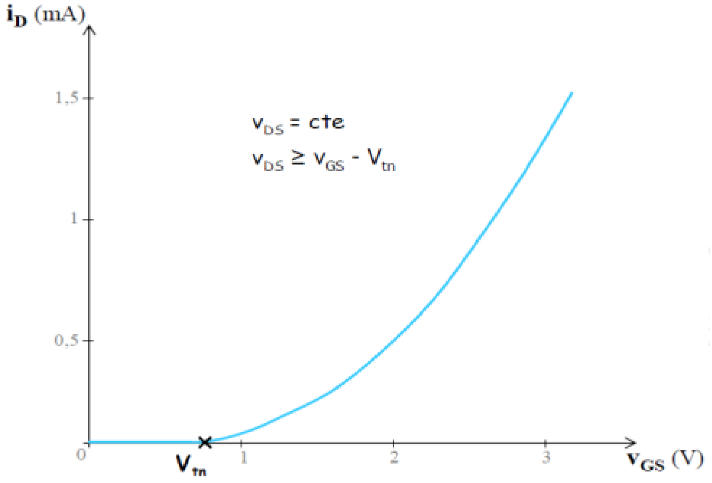


Fig I.14. I_D - V_{GS} characteristics in satureted regime

I.5 Body effect, electric field effect, channel modulation effect

I.5.1- Body effect

What is the body effect in MOSFETs, and how does it impact the threshold voltage ?

So far, we have been ignoring the substrate (or bulk or body) of the transistor and assumed that is it tied to the source **(figure no body effect)**. However, we cannot always make that assumption.

– In integrated circuits, body is common to many MOS transistors and channel is connected to most negative (positive) supply for nMOS (pMOS) transistors.

• The resulting reverse-bias voltage between the source and substrate affects device operation **(figure body effect)**.

– Reverse bias will widen the depletion region and reduces channel depth – which can be modeled as changing the threshold voltage.

The body effect in MOSFETs occurs when there is a voltage difference between the source and the substrate (bulk). This difference changes the threshold voltage of the transistor. As the source voltage becomes more positive relative to the substrate, the threshold voltage increases. This is because the depletion region between the source and the substrate widens, requiring a higher voltage to turn on the transistor.

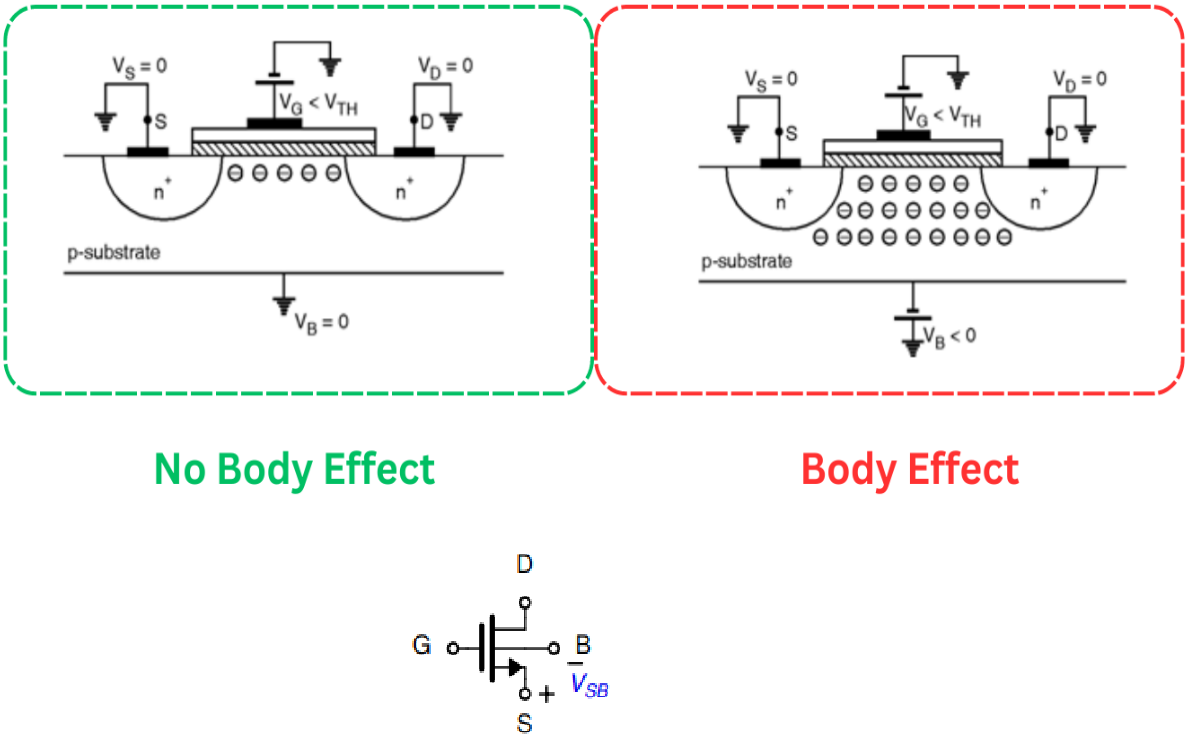


Figure.I.31 NMOS symbol with body effect

In simpler terms, the body effect means that the voltage needed to turn on a MOSFET can change based on the voltage difference between the source and the bulk. This is significant in circuits where the source voltage is not the same as the substrate voltage, leading to a variation in the threshold voltage, which can affect the performance and behavior of the circuit.

$$\boldsymbol{V_t = V_{t0} + \gamma\left[\sqrt{2\emptyset_f + V_{SB}} - \sqrt{2\emptyset_f}\right]} \qquad \text{(I.31)}$$

$$\boldsymbol{\gamma = \frac{\sqrt{2qN_a\varepsilon_s}}{C_{ox}}}$$

γ is typically 0.5.$V^{1/2}$

where :

- V_{t0}: threshold voltage at zero substrate bias ($V_{SB} = 0$)
- γ : body effect coefficient and is of 0.35 V for silicon
- ϕ_f: Fermi potential
- V_{SB}: substrate-to-source bias voltage

- ε_s: semiconductor permittivity
- *q*: electron charge
- *NA*: substrate doping concentration
- *Cox*: gate oxide capacitance per unit area

✓ As V_{SB} increases, V_t increases which affects the transistor's I-V characteristics.

- ✓ A higher body effect coefficient indicates a stronger dependence of the threshold voltage on the substrate bias
- ✓ Devices with lower substrate doping and thicker gate oxides typically have smaller body effect coefficients.

I.5.2- Electric field effect

The basic idea of the field effect transistor (FET) is to control the density of mobile electric charges by means of an electric field. When the charges are induced between two electrodes they can conduct an electric current. The structure of a FET as shown in Fig. I.32 is basically a three-terminal capacitor, where one of the two plates consists of a material which is not a conductor but allows mobile charge carriers (e.g. electrons) to exist at room temperature (such a material is also referred to as semiconductor). This plate is contacted at either end so that electrons can flow from the electron source to the drain.

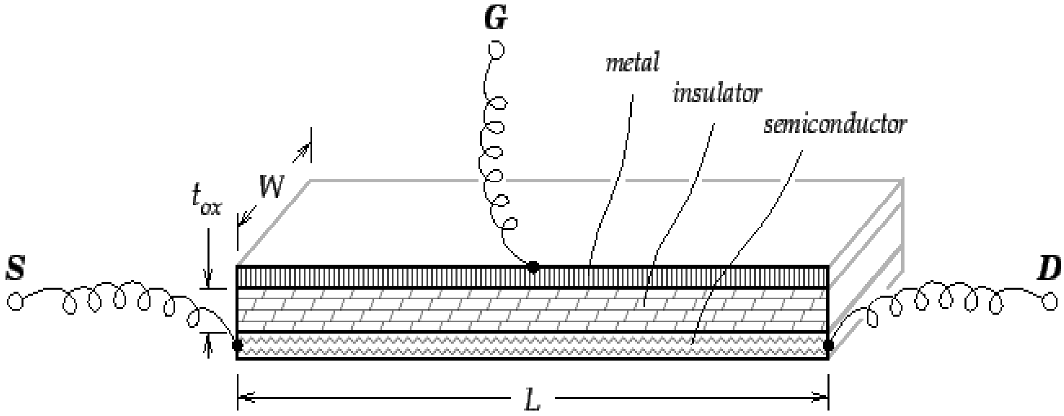


Figure I.32: Abstract field effect transistor

Normally, the mobile charge density in this plate is zero, but when a voltage $V_G > V_T$ is applied to the control gate (with $V_D = V_S = 0$ V) the vertical field $E_y = (V_G - V_T)/t_{ins}$ in the insulator with a permittivity of ε_i induces an areal charge density $Q' = \varepsilon_i(V_G - V_T)/t_{ins} = C'_{ox}(V_G - V_T)$ in the lower plate, which then forms a conducting channel between source and drain. The threshold voltage V_T is caused by fixed negative charges Q'_A in the lower plate: $V_T = t_{ins}Q'_A\,\varepsilon_s/\varepsilon_i$, where ε_s is the permittivity of the plate material. Now, when a voltage $V_D > 0$ is applied to the drain (with $V_S = 0$) a current I_D will flow through the cannel, which is controlled by the gate voltage. To calculate this current we write the charge density and the lateral field E_x as a function of the channel potential ψ (x) , where we assume that the lateral field is small compared to the vertical field, i.e., $|E_x| << |E_y|$ (gradual-channel approximation, GCA):

$$Q'(x) = C'_{ox}\big(V_G - V_T - \psi(x)\big) \quad \text{(I.32)}$$

$$E_x(x) = -\frac{d\psi(x)}{dx} \tag{I.33}$$

where :

$$C'_{ox} = \varepsilon_i / t_{ins}$$

is the capacitance per area. The current can then be written as :

$$I_D = WQ'(x)\mu E_x(x) = W\mu C'_{ox}\big(V_G - V_T - \psi(x)\big)\frac{d\psi(x)}{dx}, \tag{I.34}$$

where μ is the charge carrier mobility. Integrating (I.34) from *x*=0 to *L* finally gives

$$I_D = \frac{W}{L}\mu C'_{ox}\left((V_G - V_T)V_D - \frac{V_D^2}{2}\right), \tag{I.35}$$

which holds for $V_D < V_G - V_T$. As the current varies linarly with the control voltage V_G this is also called the linear region of operation. As the channel potential rises towards the drain the charge density decreases, i.e., the channel gets thinner at the drain side.

When $V_D > V_G - V_T$ the charge density $Q'(x)$ would approach zero before the drain at some $x = L' < L$ which is called the pinch-off point, requiring an infinite lateral field to maintain the current. However, the model loses its validity before this point as the lateral field was assumed to be small compared to the vertical one. Further analysis of Poisson's equation without the gradual-channel approximation, i.e., including a term $\varepsilon_s \partial^2\psi/\partial x^2$

in the charge density does not lead to an analytical current expression, but it shows that both E_x and Q' remain finite and the current saturates at about

$$I_D = \frac{W}{L}\frac{\mu C'_{ox}}{2}(V_G - V_T)^2, \tag{I.36}$$

The channel length modulation L'/L is neglected. Therefore, this operating region is also called the saturation region.

(I.35) and (I.36) are most widely used throughout literature. Yet, whenever using these equations it should be kept in mind that they were derived from the rather simple structure in Fig. I.32, which may not reflect the physical behavior of the considered devices.

I.5.3- Channel modulation effect

Channel length modulation (CLM) is an effect in field effect transistors, a shortening of the length of the inverted channel region with increase in drain bias for large drain biases. The result of CLM is an increase in current with drain bias and a reduction of output resistance. It is one of several short-channel effects in MOSFET scaling. It also causes distortion in JFET amplifiers.

The channel gets pinched-off only when the MOSFET reaches saturation, beyond which only channel length modulation has direct effect on the drain current. This is because channel length modulation reduces the effective channel length by ΔL afterwards.

Now for the ideal case, in the saturation region, I_{DS} becomes independent of V_{DS} i.e. in the saturation region channel is pinched off at the drain end and a further increase in V_{DS} has no effect on the channel's shape. But in practice increase in V_{DS} does affect the channel. In the saturation region, when V_{DS} increases, the channel pinch-off point is moved slightly away from the drain, towards the source as the drain electron field "pushes" it back. The reverse bias depletion region widens and the effective channel length decreases by an amount of ΔL for an increase in V_{DS}. Thus the channel no longer "touches" the drain and acquires an asymmetrical shape that is thinner at the drain end. This phenomenon is known as channel length modulation.

« Thus channel length modulation can be defined as the change or reduction in length of the channel (L) due to increase in the drain to source voltage (V_{DS}) in the saturation region ».

In large devices, this effect is negligible but for shorter devices $\Delta L/L$ becomes important. Also in the saturation region due to channel length modulation, I_{DS} increases with increase in V_{DS} and also increases with the decrease in channel length L.

The voltage-current curve is no longer flat in this region.

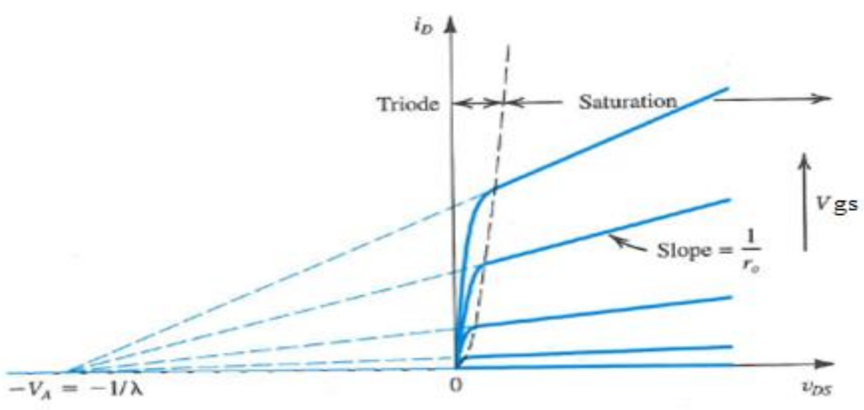


Fig I.33: The channel-length modulation effect causes the iD-vDS characteristics to change for different Vgs

The drain current with channel length modulation is given by:

$$I_{DS} = I_D = I_{Dsat}\,(1 + \lambda V_{DS}) \tag{I.37}$$

To account for the dependence of I_D on V_{DS} in the saturation region, replace L by L – ΔL. We know that in the saturation region, drain to source current ($I_{DS} = I_D$) is given by:

$$I_D = \frac{kW}{2L}(V_{GS} - V_T)^2 \tag{I.38}$$

$$I_D = \left(\frac{k}{2}\right)\left(\frac{W}{L-\Delta L}\right)(V_{GS} - V_T)^2 \tag{I.39}$$

$$I_D = \left(\frac{k}{2L}\right)\left(\frac{W}{L-\frac{\Delta L}{L}}\right)(V_{GS} - V_T)^2 \tag{I.40}$$

Assuming (ΔL/L) < 1

$$I_D = \left(\frac{kW}{2L}\right)\left(L + \frac{\Delta L}{L}\right)(V_{GS} - V_T)^2 \tag{I.41}$$

Since ΔL increases with increase in V_{DS}

$$\Delta L \propto V_{DS} \qquad \text{or} \qquad \Delta L = \lambda' V_{DS} \tag{I.42}$$

where, λ' : is process technology parameter with unit *µm/V.*

$$I_D = \left(\frac{kW}{2L}\right)\left(1 + \frac{\lambda' V_{DS}}{L}\right)(V_{GS} - V_T)^2 \tag{I.43}$$

Therfore :

$$I_{DS} = I_D = I_{Dsat}\,(1 + \lambda V_{DS}) \tag{I.44}$$

Where, λ'/L = λ = process technology parameter with unit µm/V.

$$I_{DSat} = \left(\frac{kW}{2L}\right)(V_{GS} - V_T)^2 \quad (I.45)$$

$$V_{DS} = -1/\lambda = V_A \quad \text{(Early tension)} \quad (I.46)$$

V_A est un paramètre valant typiquement 100 à 300V.

As a result, the output resistance of the MOSFET operating in the saturation region is finite and can be expressed as:

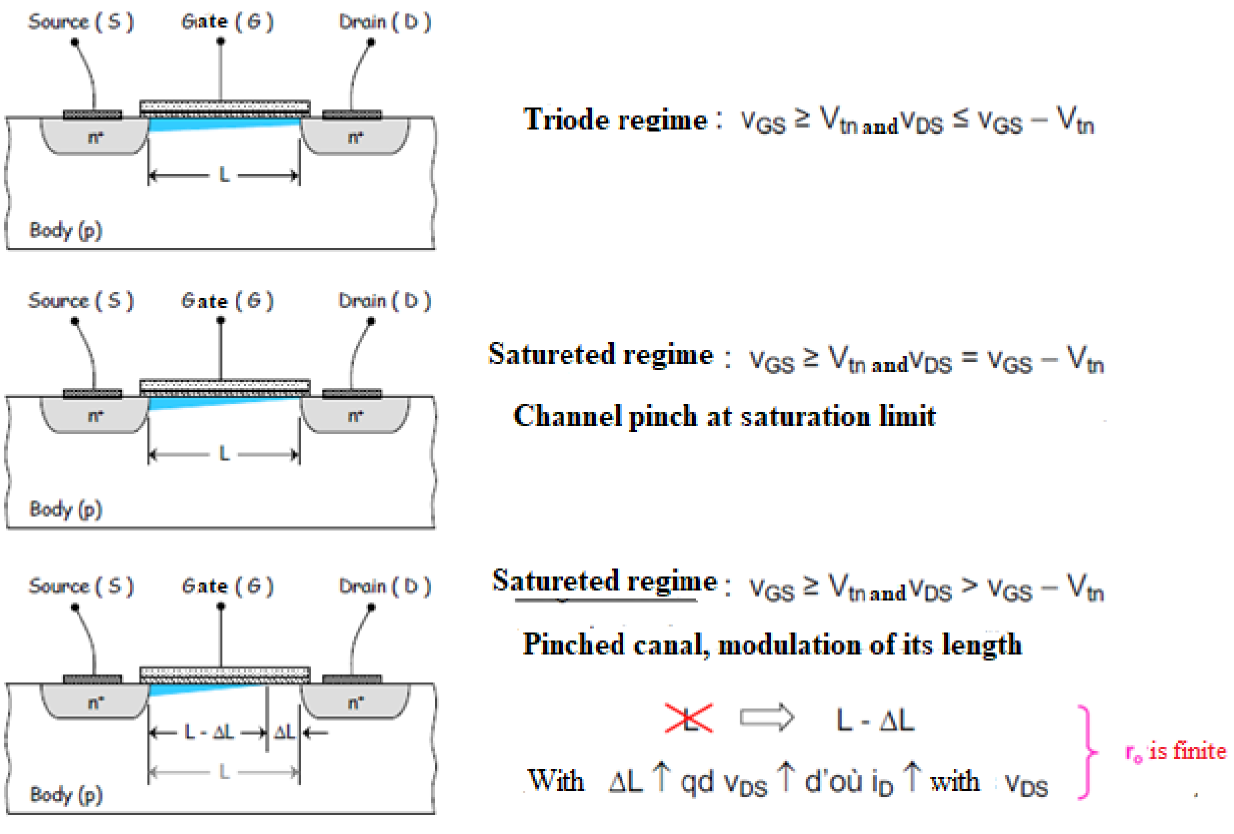


Fig.I.34 Cross-sectional view of an n-channel (nMOS) transistor, (a) operating in the linear region, (b) operating at the edge of saturation, and (c) operating beyond saturation.

I.6 Pspice model of the MOS transistor

The SPICE circuit analysis program is used to simulate more complicated circuits and to make much more detailed calculations than we can perform by hand analysis. The circuit representation for the MOSFET model that is implemented in SPICE is given in Fig.I.35, and as we can observe, the model uses quite a number of circuit elements in an attempt to accurately represent the characteristics of a real MOSFET. For example, small resistances *RS* and *RD* appear in series with the external MOSFET source and drain terminals, and diodes are included between the source and drain regions and the substrate.

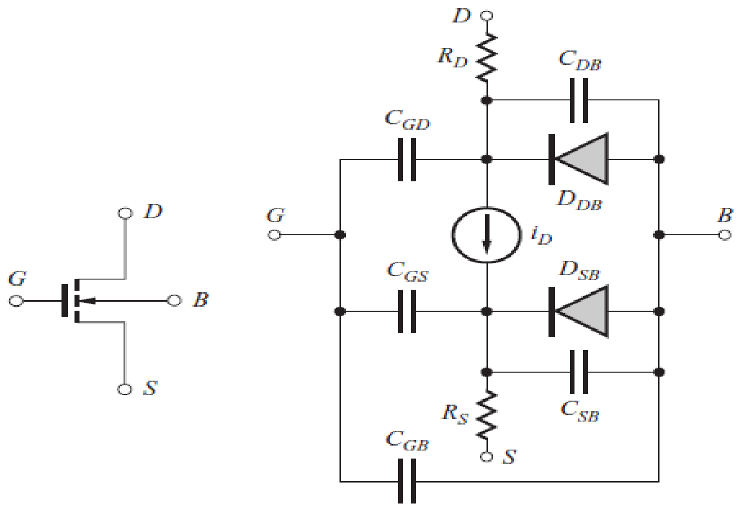


Fig.I.35 SPICE model for the NMOS transistor.

As many as 20 different MOSFET models of varying complexity are built into various versions of the SPICE simulation program, and they are denoted by "Level=Model Number". The levels each have a unique mathematical formulation for current source ID and for the various device capacitances. The model we have studied in this chapter is the most basic model and is referred to as the Level-1 model (LEVEL=1). The LEVEL=1 model is coded into SPICE using the following formulas, which are the similar to those we have already studied.

Table I.3 contains the equivalences of the SPICE model parameters . Typical and default values of the SPICE model parameters can be found in Table I.3. A similar model is used for the PMOS transistor, but the polarities of the voltages and currents, and the directions of the diodes, are reversed.

$$\text{Triode region:} \quad i_D = \text{KP}\frac{W}{L}\left(v_{GS} - \text{VT} - \frac{v_{DS}}{2}\right)v_{DS}(1 + \text{LAMBDA} \cdot v_{DS})$$

$$\text{Saturation region:} \quad i_D = \frac{\text{KP}}{2}\frac{W}{L}(v_{GS} - \text{VT})^2(1 + \text{LAMBDA} \cdot v_{DS})$$

$$\text{Threshold voltage: } \text{VT} = \text{VTO} + \gamma\left(\sqrt{v_{SB} + \text{PHI}} - \sqrt{\text{PHI}}\right) \tag{I.47}$$

Notice that the SPICE level-1 description includes the addition of channel-length modulation to the triode region expression. Also, be sure not to confuse SPICE threshold voltage V_T with thermal voltage V_T .

Table I.3 Equivalences of the SPICE model parameters

SPICE Parameter Equivalences

PARAMETER	OUR TEXT	SPICE	DEFAULT
Transconductance	K'_n or K'_p	KP	20 $\mu A/V^2$
Threshold voltage	V_{TN} or V_{TP}	VT	—
Zero-bias threshold voltage	V_{TO}	VTO	1V
Surface potential	$2\phi_F$	PHI	0.6 V
Body effect	γ	GAMMA	0
Channel length modulation	λ	LAMBDA	0
Mobility	μ_n or μ_p	UO	600 $cm^2/V \cdot s$
Gate-drain capacitance per unit width	C_{GDO}	CGDO	0
Gate-source capacitance per unit width	C_{GSO}	CGSO	0
Gate-bulk capacitance per unit length	C_{GBO}	CGBO	0
Junction bottom capacitance per unit area	C_J	CJ	0
Grading coefficient	MJ	MJ	0.5 $V^{0.5}$
Sidewall capacitance	C_{JSW}	CJSW	0
Sidewall grading coefficient	MJSW	MJSW	0.5 $V^{0.5}$
Oxide thickness	T_{ox}	TOX	100 nm
Junction saturation current	I_S	IS	10 fA
Built-in potential	ϕ_J	PB	0.8 V
Ohmic drain resistance	—	RD	0
Ohmic source resistance	—	RS	0

The junction capacitances Cj are modeled in SPICE by a generalized form of the capacitance expression in (I.49).

$$C_J = \frac{CJO}{\left(1+\frac{v_R}{PB}\right)^{MJ}} \quad \text{and} \quad C_{JSW} = \frac{CJSWO}{\left(1+\frac{v_R}{PB}\right)^{MJSW}} \qquad (I.48)$$

The capacitance of the reverse-biased *pn* junction is given by :

$$C_j = \frac{dQ_n}{dv_R} = \frac{C_{jo}A}{\sqrt{1+\frac{v_R}{\phi_j}}} \quad \text{where } C_{jo} = \frac{\varepsilon_s}{w_{do}} \quad F/cm^2 \qquad (I.49)$$

where *A* is the cross-sectional area of the diode and *wd* is described by (I.50) in which *Cjo* represents the **zero-bias junction capacitance** per unit area of the diode. Equation (I.49) shows that the capacitance of the diode changes with applied voltage. The capacitance decreases as the reverse bias increases, exhibiting an inverse square root relationship.

$$w_d = w_{do}\sqrt{1+\frac{v_R}{\phi_j}} \qquad \text{where } w_{do} = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)\phi_j} \tag{I.50}$$

SPICE has four MOS transistor models:

1) Level 1 model (LEVEL = 1): Shichman and Hodges quadratic type, this is the default model.

2) Level 2 model (LEVEL = 2): This is an analytical model that takes into account second-order and small-scale effects.

3) Level 3 model (LEVEL = 3): A semi-empirical model particularly intended for very small MOS transistors.

4) Level 4 model (LEVEL = 4): Related to manufacturing process parameters.

I.6.1 Describing MOSFETs To Spice

MOSFETs are described to Spice using two statements; one statement describes the nature of the FET and its connections to the rest of the circuit, and the other specifies the values of the parameters of the built-in FET model. The following outlines the syntax of these two statements, including some details on the built-in ``Level 1" MOSFET model of Spice.

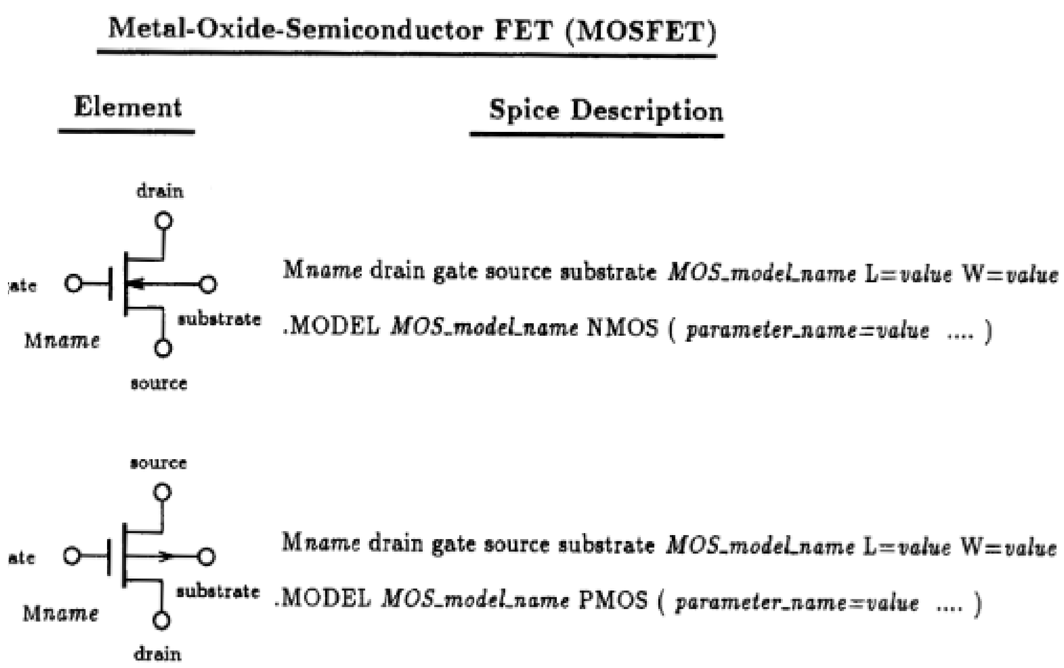


Fig. I.36: Spice element description for the NMOS and PMOS MOSFETs.

Also listed is the general form of the associated MOSFET model statement. A partial listing of the parameter values applicable to either the NMOS or PMOS MOSFET is given in Table I.4. Enhancement or depletion mode of operation is determined by the values assigned to these parameters.

Table. I.4: A partial listing of the Spice parameters for the LEVEL 1 MOSFET model.

Symbol	Spice Name	Model Parameter	Units	Default
	Level	Model type		1
μC_{OX}	kp	Transconductance coefficient	A/V^2	20μ
V_{t0}	Vto	Zero-bias threshold voltage	V	0
λ	lambda	Channel-length modulation	V^{-1}	0
γ	gamma	Body-effect parameter	$V^{1/2}$	0
$2\phi_f$	phi	Surface potential	V	0.6
r_D	Rd	Drain ohmic resistance	Ω	0
r_S	Rs	Source ohmic resistance	Ω	0

I.7 Method for simulating the characteristics of a MOS transistor using Pspice

- **Simulation**

In the simulation section, create the diagrams by following the steps:

a- Open Orcad Capture CIS

b- Click on “File” and New Project

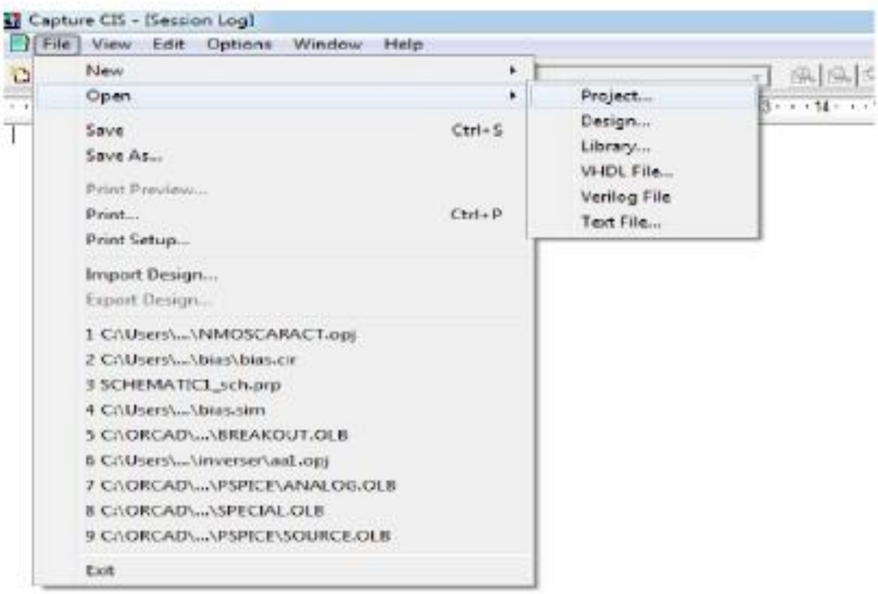


Fig.I.36

c- Give a name and click on “ok”

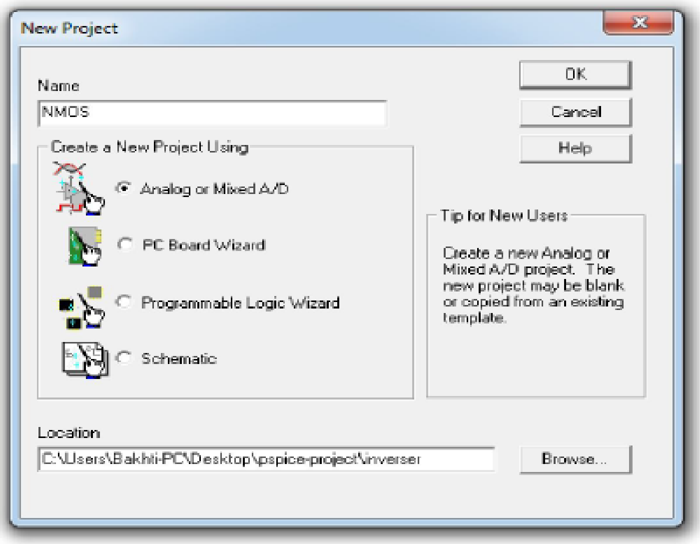


Fig.I.37

d- Select “Create Blank Project” and click “OK”

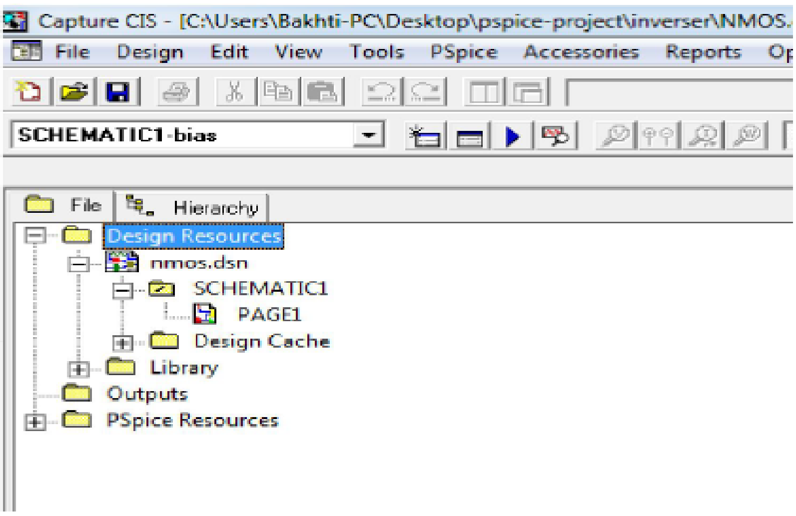
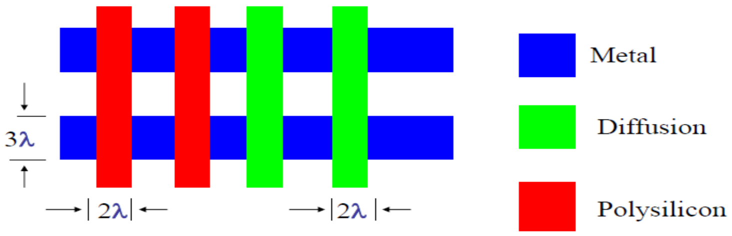


Fig I.38

e - Take the necessary components from PSPICE library and click on “OK”



- **PolySi–PolySi space 2λ**
- **Metal-Metal space 2λ**

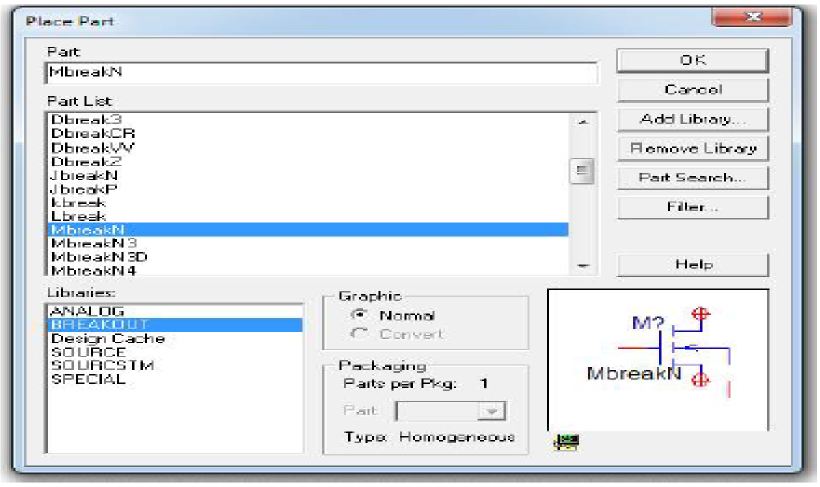


Fig.I.39

f- Connect the components with « wire »

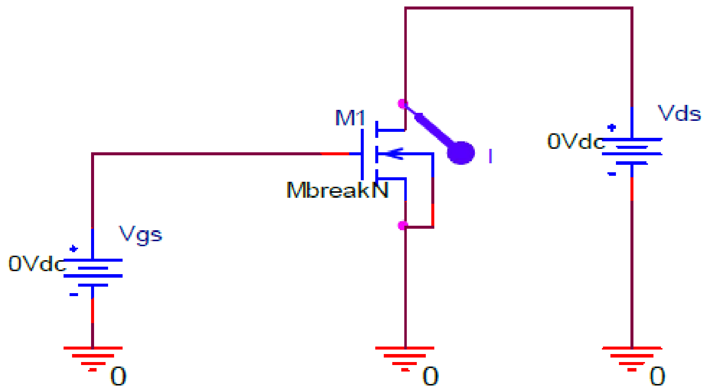


Fig I.40

g- Configured the Continuous sources by clicking PSPICE menu

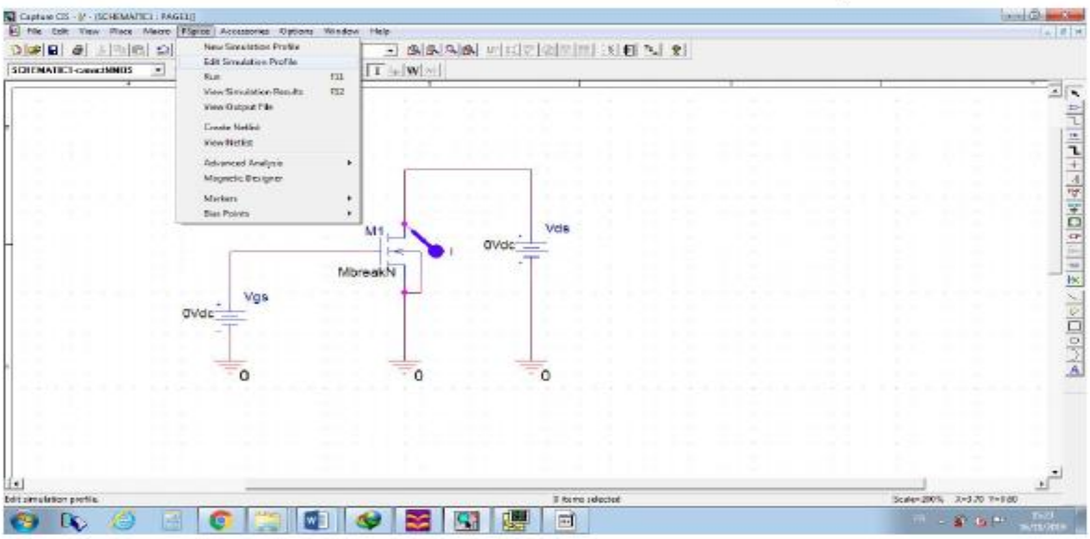


Fig I.41

• **Diffusion- Diffusion space 3λ**

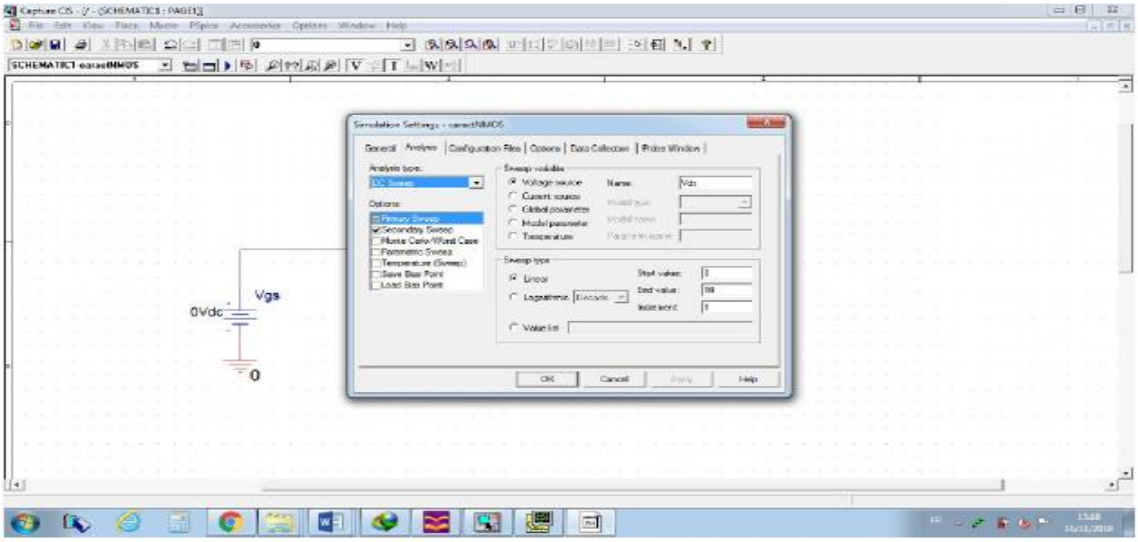


Fig I.42

h-Simulation

If there are no design errors, we will have curves Ids = f(Vds) similar to the one in the figure below.

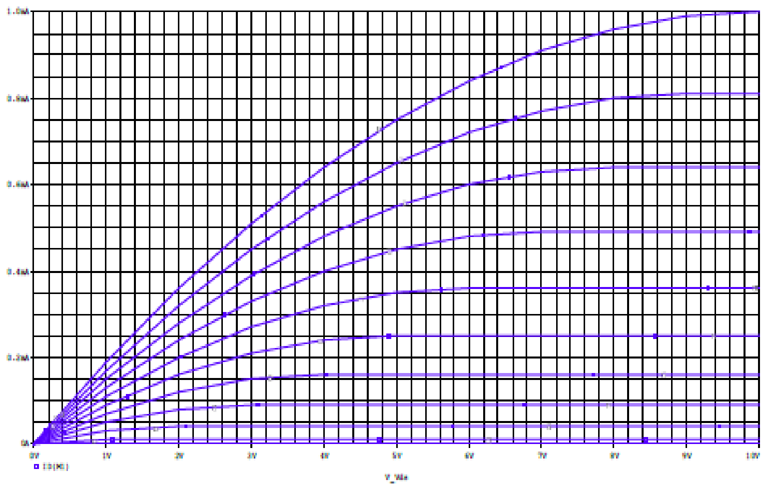


Fig I.44 characteristic Ids = f(Vds)

i- Question

A - Analyze the characteristic Ids = f(Vds) and calculate the resistance of the ohmic part for each voltage Vgs. What can we conclude from this?

B - Plot and discuss the characteristic Ids = f(Vgs).

C- Study the effect of the shape on the transistor characteristic (L, W, Kp, Kn).

D- Repeat the same task with a PMOS transistor.

I.8 Exercises

<u>Exercices 1</u> : Consider an N-channel MOSFET (NMOS) whose characteristics are :

V_T = 0.75V ; W = 40um ; L = 4um ; μ_n = 650 cm^2/V.s ; t_{ox} = 450.10^{-10} m ; $\varepsilon_0\varepsilon_{ox}$ = 8.85.10^{-14}.3.9 F/cm. We propose to calculate the current in saturation regime and for $V_{GS} = 2.V_T$.

<u>Solution</u> 1: in saturation regime the expression of the current is given by the relation :

$$I_{Dsat} = K_n.(V_{GS} - V_T)^2$$

$$K_n = \mu_{n.}C_{ox}.\frac{W}{2L}$$

$$\boldsymbol{C_{ox}} = \frac{\varepsilon_0\varepsilon_{ox}}{t_{ox}} = \frac{8.85\times10^{-14}\times3.9}{450\times10^{-10}} \;\; ; \; \boldsymbol{C_{ox} = 7.67\ \mu m}$$

$$K_n = 650 \times 7{,}67 \times 10^{-6}.\frac{4}{2\times40} \; ; \boldsymbol{K_n = 0.249\ mA/V^2}$$

$$I_D = 0.249 \times (0.75)^2 \; ; \quad \boldsymbol{I_D = 0.14\ mA}$$

<u>Exercice 2</u> : Consider an NMOS fabricated in a 0.18-um process with L= 0.18 um and W = 2um.The process technology is specified to have Cox = 8.6 fF/um^2 ,μ_n = 450 cm^2/V.s, and Vtn = 0.5V. Find V_{GS} and V_{DS} that resullt in the MOSFET operating at the edge of saturation with I_D = 100uA.

<u>Solution :2</u>

First we determine the process transconductance parameter :

$k'_n = \mu_n.C_{ox} = 450\times10^{-4} \times 8.6\times10^{-15}\times10^{12}$ A/V^2 = **387uA/V^2**

and the transistor transconductance parameter k_n , $k_n = k'_n$ (W/L) = 387. (2/0.18) = **4.3mA/ V^2**

with the transistor operating in saturation,

$$I_D = (1/2)\ k_n.(V_{GS}-V_{tn})^2$$

Thus, $100 = (1/2) \times 4.3\times10^{-3}\times(V_{GS}-V_{tn})^2$

witch result in $(V_{GS}-V_{tn}) = 0.22V$

Thus $V_{GS} = 0.22 + V_{tn} = 0.22 + 0.5 =$ **0.72V**

and since operation is at the edge of saturation,

$$V_{DS} = V_{GS}-V_{tn} = \mathbf{0.22V}$$

For $V_{DS} \geq V_{DSsat}$, the pinch point moves towards the source by a length ΔL. The channel remains under tension V_{DSsat} , excess voltage (V_{DS} - V_{DSsat}) is established at the limits of the S.C.Z. The drain current substantially retains its value I_{DSsat} except for short channels where the decrease in length of the quantity ΔL not negligible in front L, causes a variation in the conductance resulting in an increase in the drain current which can be expressed by :

$$I_D = I_{DSsat}.\frac{1}{1-\frac{\Delta L}{L}}$$

Exercise 3: What are the values of SPICE model parameters KP, LAMBDA, VTO, PHI, *W*, and *L* for a transistor with the following characteristics: V_{TN} = 1V, K_n = 150µA/V^2, *W* = 1.5µm, *L* = 0.25µm, λ = 0.0133 V^{-1}, and $2\varphi_F$ = 0.6 V?

Solution 3: 150 µA/V2; 0.0133 V^{-1}; 1 V; 0.6 V; 1.5 µm; 0.25 µm (specified in SPICE as 150u ; 0.0133; 1; 0.6; 1.5u; 0.25u).

Conclusion

This chapter enables the reader to master the theoretical and practical foundations of the MOS transistor. Understanding the physical and electrical models, combined with simulation via PSpice, forms an indispensable basis for designing complex MOS circuits.

Chapter II : Basic analog circuits using MOS technology

Introduction

This chapter demonstrates how MOS transistors can be used to implement essential analog circuits such as current mirrors, level shifters, common-source amplifiers, differential amplifiers, and operational amplifiers. The analysis of each structure is rigorous, combining theory, analytical equations, and schematic representations.

II.1 Current mirrors: analysis of the different types of current mirrors

II.1.1 The current mirror function (Simple current mirror)

Objective ⇒ constant current and independent of circuit parameters and voltages.

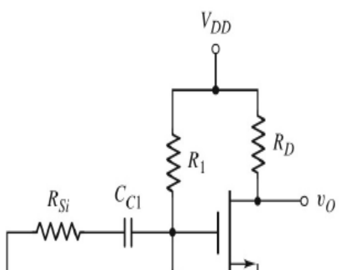
Several possible uses:

- Current sources
- Static transistor biasing
- Active load (synthesis of high-value virtual resistors) *f*
- Changing the signal attachment point

The simple current mirror is the basic element used for replication, addition is the subtraction of current. It only works with unipolar current. Considering the current mirror consisting of two MOS transistors shown in Figure III.4.

The parameters of the circuit shown in Figure Q1 are V_{DD} = 5 V, $R1$ = 520 kΩ, $R2$ = 320 kΩ, R_D = 10 kΩ, and R_{Si} = 0. Assume transistor parameters of V_{TN} = 0.8 V, K_n = 0.20 mA/V^2, and λ= 0.

(a) Determine the small-signal parameters g_m and r_o.



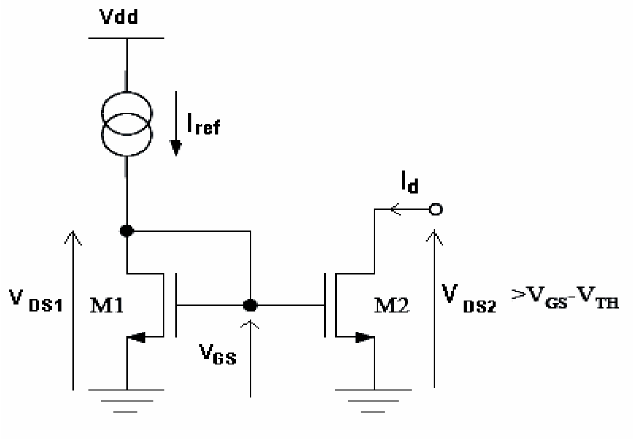


Fig II.1 Simple current mirror

The current mirror uses the following principle: if the gate-source potentials V_{GS} of two MOS transistors M1 and M2 are identical, the currents flowing in their respective channels must be equal for the saturation regime (high Vds).

Let I_{ref} be the input current and I_d the output current, also called the image of I_{ref}

$$V_{DS1} = V_{GS} \quad \text{(II.51)}$$

Assuming that :

$$V_{DS2} \geq V_{GS} - V_{th} \quad \text{(II.52)}$$

So V_{DS2} is greater than (Vth) with this statement allows the use of the equations of two transistors in the saturation regime:

$$\begin{aligned} I_{ref} &= \frac{1}{2}\mu_1 C_{ox1}\frac{W_1}{L_1}(V_{GS} - V_{th1})^2(1+\lambda V_{DS1}) \\ I_d &= \frac{1}{2}\mu_2 C_{ox2}\frac{W_2}{L_2}(V_{GS} - V_{th2})^2(1+\lambda V_{DS2}) \end{aligned} \quad \text{(II.53)}$$

μ_1 and μ_2 : electron mobilities of transistors M1 and M2,

C_{ox1}, C_{ox2} : Capacité de l'oxyde mince (grille),

I_{ref} : Courant de référence,

I_d : Courant de drain de transistor M2,

W1, L1, W2, L2 : les dimensions géométriques de deux transistors M1, M2,

λ : Coefficient de modulation de longueur du canal en V^{-1},

V_{th1}, V_{th2} : Les tensions de seuil de deux transistors M1, M2,

V_{GS} : La tension d'entrée grille-source,

V_{DS1}, V_{DS2} : La tension de sortie drain-source de deux transistors M1, M2.

The report $\frac{I_d}{I_{ref}}$ is given by : $\frac{I_d}{I_{ref}} = \left(\frac{L_1 W_2}{L_2 W_1}\right)\left(\frac{V_{GS} - V_{th2}}{V_{GS} - V_{th1}}\right)^2 \left(\frac{1+\lambda V_{DS2}}{1+\lambda V_{DS1}}\right)\left(\frac{\mu_2 C_{ox2}}{\mu_1 C_{ox1}}\right)$ (II.54)

For current mirror components fabricated in the same integrated circuit, the physical parameters such as V_{th}, C_{ox}, μ are identical for both transistors so we can simplify the equations:

$$\frac{I_d}{I_{ref}} = \left(\frac{L_1 W_2}{L_2 W_1}\right)\left(\frac{1+\lambda V_{DS2}}{1+\lambda V_{DS1}}\right) \quad \text{(II.55)}$$

Finally, if $V_{DS1} = V_{DS2}$, the report $\frac{I_d}{I_{ref}}$ becomes : $\frac{I_d}{I_{ref}} = \left(\frac{L_1 W_2}{L_2 W_1}\right)$ (II.56)

II.2 Shift circuit

Bidirectional Logic Level Shifter Circuit

A logic level shifter, or a voltage level translator, is used to translate signals from one logic level to another. Nowadays, most of the system runs on 3.3V or 5V. Logic level is simply a HIGH and LOW level of voltage for a certain board or IC. Knowing this, a logic level shifter is necessary to create a path between processors, sensors, or boards of different voltage levels.

A simple bidirectional logic level shifter is built around a single transistor and, as the switching speed is not an issue, is a very handy and convenient circuit.

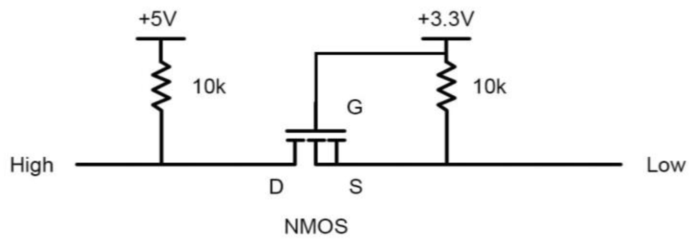


Fig.II.2

When HIGH (pin) is logic1 (i.e., 5V at that pin), the drain and source of the MOSFET are pulled high. Gate voltage will be lower than the source voltage in this case and so MOSFET is in the cut-off region (i.e., inactive). Thus, the LOW pin is pulled at 3.3V as no current flows through the gate. When HIGH is logic0, the gate voltage is greater than the source voltage which will pull the LOW pin output down.

Similarly, when LOW is logic1, then Vgs (gate-source voltage) will be 0 and so the transistor will be inactive pulling the HIGH pin to +5V. When LOW is logic0, the gate voltage is again higher than the source voltage and the HIGH pin is pulled down.

II.3 Common source amplifier

The amplification function (Simple Amplifier)

"Common source" assembly: let's replace the drain resistor with an NMOS transistor (M2).

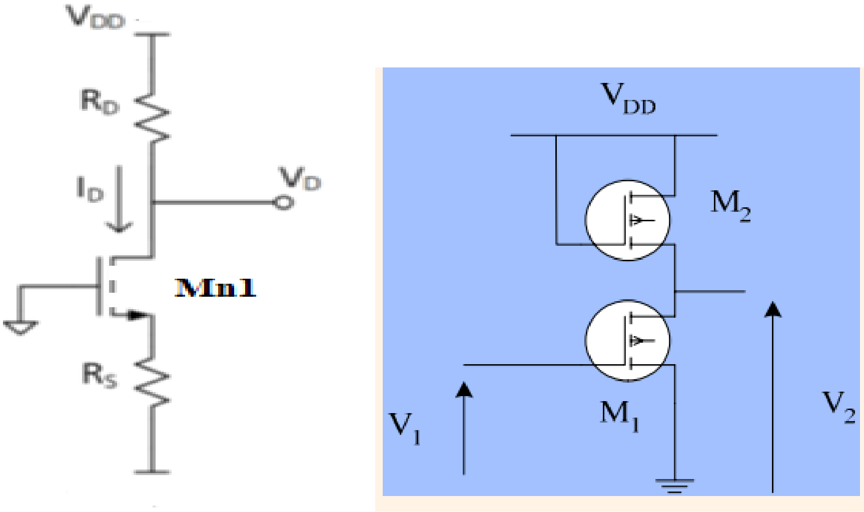


Fig II.3 Simple MOS Amplifier

<u>Voltage transfer characteristic</u>: We are in the context of the 2 Transistors in saturated mode.

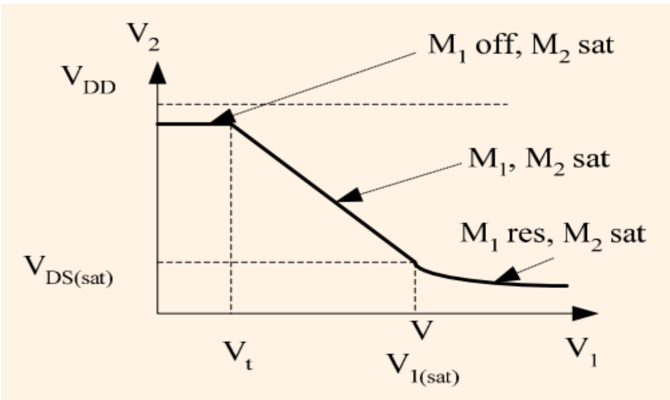


Fig. II.3 Voltage transfer characteristic

$$I_{D1} = \mu_n C_{ox} \frac{W_1}{2L_1}(V_1 - V_t)^2 = I_{D2} = \mu_n C_{ox} \frac{W_2}{2L_2}(V_{DD} - V_2 - V_t)^2 \qquad \text{(II.57)}$$

which gives for the output voltage : $$V_2 = V_{DD} - V_t - \sqrt{\frac{W_1/L_1}{W_2/L_2}}(V_1 - V_t) \qquad \text{(II.58)}$$

Let's say a dynamic gain in voltage: $$A_V = \frac{dV_2}{dV_1} = -\sqrt{\frac{W_1/L_1}{W_2/L_2}} \qquad \text{(II.59)}$$

<u>Approach Small signals:</u> :

(b) Find the small-signal voltage gain *vo*/*vi*.

(c) Calculate the input and output resistances *R*i and *R*o.

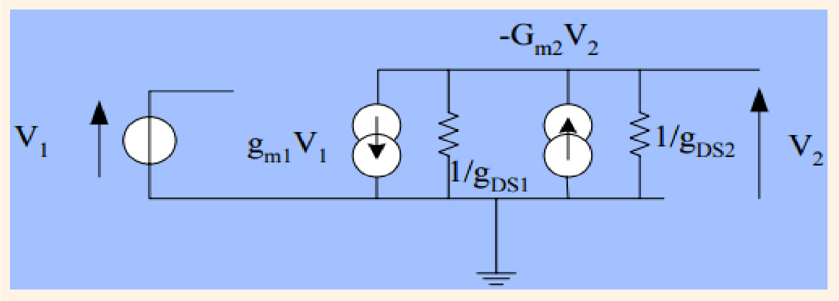


Fig II.4 Small signal diagram of a MOS amplifier

The law of output nodes : $$g_{m1}V_1 + g_{m2}V_2 + \frac{V_2}{1/g_{ds1}} + \frac{V_2}{1/g_{ds2}} = 0 \quad \text{(II.60)}$$

Let the voltage gain be: $$A_V = \frac{V_2}{V_1} = -\frac{g_{m1}}{g_{m2} + g_{ds1} + g_{ds2}} \quad \text{(II.61)}$$

Output resistance: $$R_S = \frac{1}{g_{m2} + g_{ds1} + g_{ds2}} \quad \text{(II.62)}$$

II.4 Differential amplification

The differential amplification function (The MOS differential pair)

The objective : of this differential amplifier is to compare two analog signals and amplify their difference. It is one of the most important building blocks of electronics.

Interest :

- High immunity to noise and interference,
- Ease of polarization,
- Better linearity.

An electrical signal is usually measured relative to ground (i.e. a fixed potential):

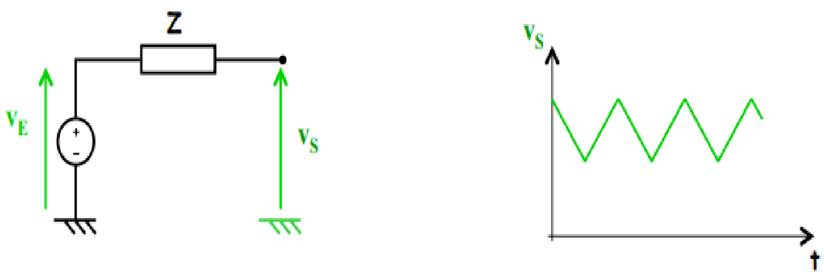


Fig.II.5

A differential signal is measured between two nodes having equal and opposite voltage excursions with respect to a fixed potential (the common mode):

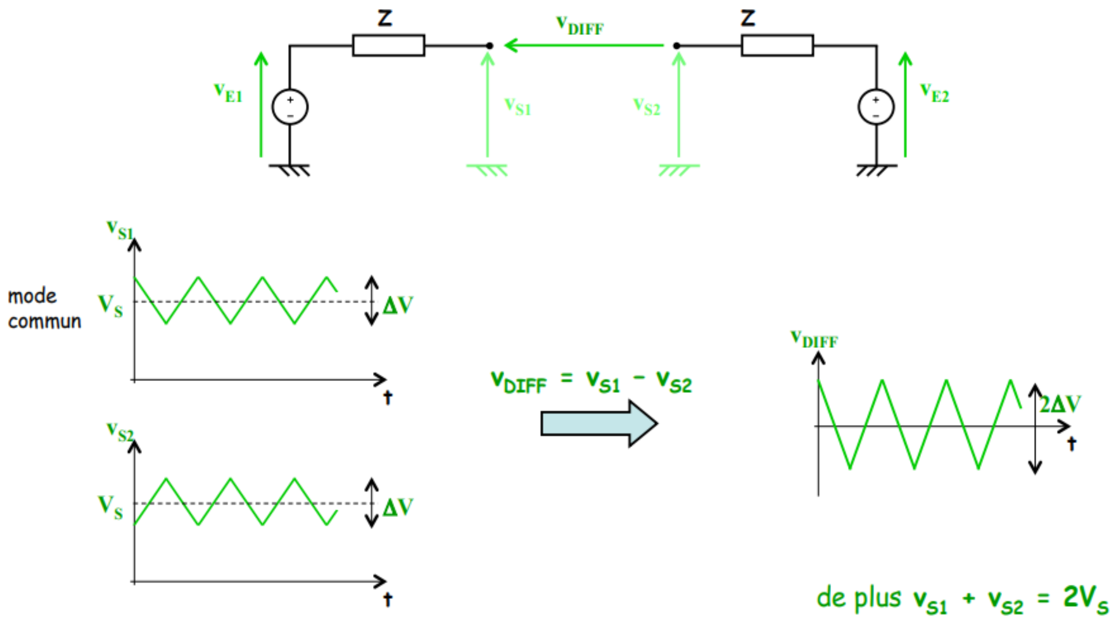


Fig.II.6

The MOS differential pair

a- Presentation :

- ✓ Mn1 and Mn2 are identical
- ✓ Vertical axis of symmetry
- ✓ Polarization by an ideal current source ($r0= \infty$) and polarized in saturated mode.

Objectives :

- ✓ Amplify the difference between 2 signals
- ✓ Do not amplify the average value of the same 2 signals

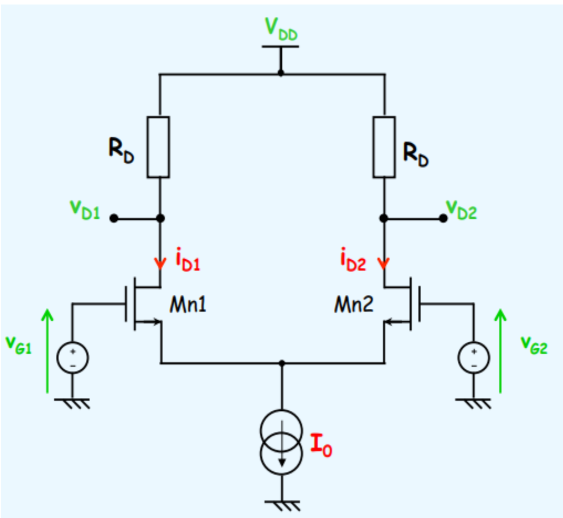


Fig II.7 MOS-based differential pair

b- Operation with a common mode input voltage

$$\Rightarrow V_{G1} = V_{G2} = V_{CM} \qquad \text{(II.63)}$$

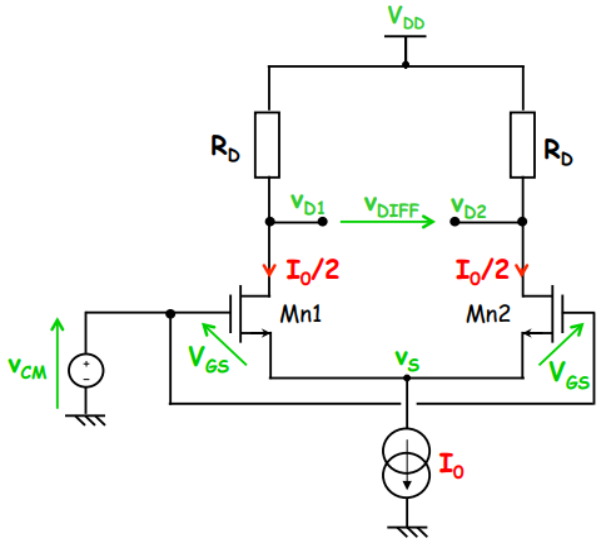


Fig.II.8

According to Mn1 and Mn2 identical and by considerations of symmetry:

$$I_{D1} = I_{D2} = I_0/2 \qquad \text{(II.64)}$$

We have : $V_S = V_{CM} - V_{GS}$ such as :

$$\frac{I_0}{2} = \frac{1}{2} k_n \frac{W}{L} (V_{GS} - V_{tn})^2 \qquad \text{(II.65)}$$

Let: $$V_{OV} = \sqrt{I_0 / k_n (W/L)} \qquad \text{(II.66)}$$

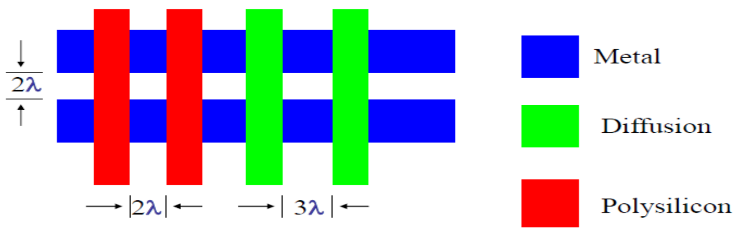
At the drain level: $$V_{D1} = V_{D2} = V_{DD} - \frac{I_0}{2} R_D \qquad \text{(II.67)}$$

➡ The output differential voltage: $$V_{Diff} = V_{D2} - V_{D1} = 0 \qquad \text{(II.68)}$$

The differential pair does not respond to a common mode input signal, we speak of common mode rejection (in the presence of faults such that Mn1≠Mn2 this is no longer true).

Figure Q1

Solution 2:



• **Diffusion space-PolySi λ** to prevent lines from overlapping to form an unwanted capacitor

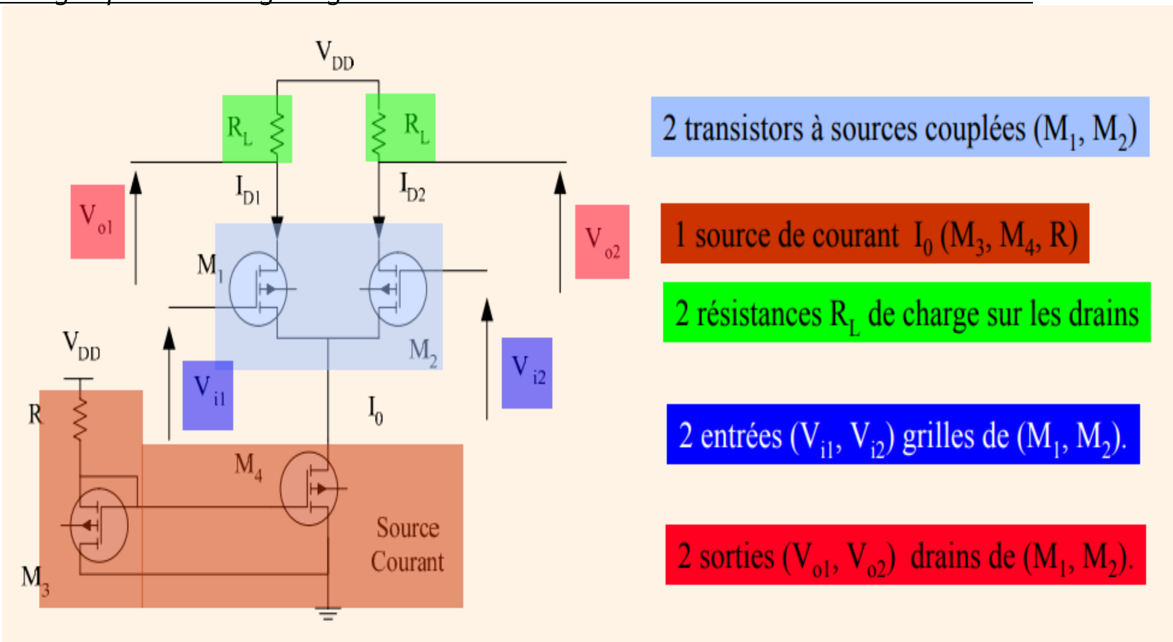


Fig.II.9

c- Differential Mode and Common Mode:

$V_{id} = V_{i1} - V_{i2}$ Differential $V_{od} = V_{o1} - V_{o2}$

$V_{ic} = \frac{V_{i1} + V_{i2}}{2}$ Common $V_{oc} = \frac{V_{o1} + V_{o2}}{2}$

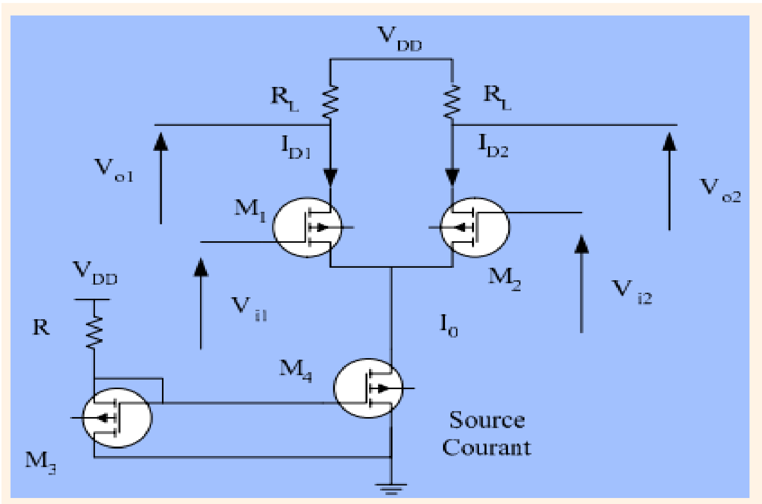
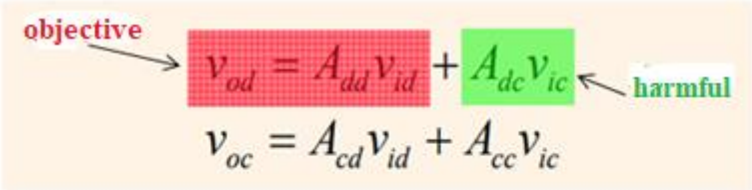


Fig.II.10

Gain equation of the differential pair:

$$V_{od} = A_{dd} V_{id} + A_{dc} V_{ic} \quad \text{(II.69)}$$

• The metal lines can pass through both the diffusion and the polySi without any electrical effect. Where no separation is specified, the metal lines may overlap or cross.



(II.70)

d- Common Mode Rejection Ratio

$$TRMC = 20\log_{10}\left(\frac{A_{dd}}{A_{dc}}\right) \cong 60dB \qquad (II.71)$$

Differential Mode Gain A_{DD}

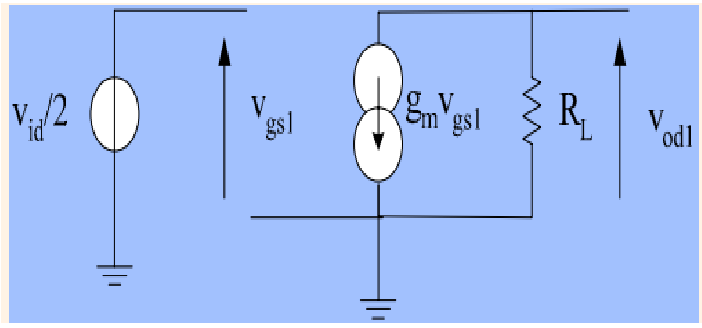


Fig.II.11

M1 and M2 identical ⇒ Symmetrical assembly
I0 constant ⇒ virtual ground

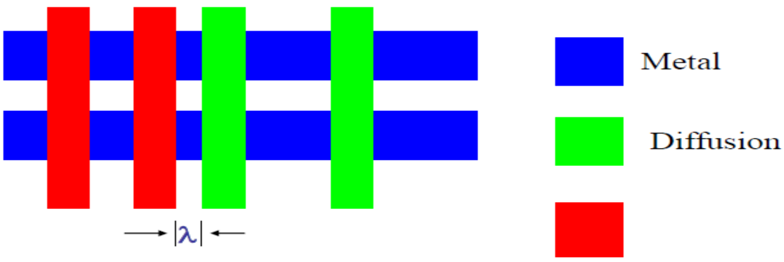
Neglect:

- ✓ Drain-Source resistance 1/gDS
- ✓ Parasitic capacitances.

We obtain:: $$V_{od} = -\frac{g_m R_L}{2} V_{id} \qquad (II.72)$$

Let globally : $$A_{dd} = \frac{V_{od}}{V_{id}} = -g_m R_L \qquad (II.73)$$

A_{DC} Common Mode Gain



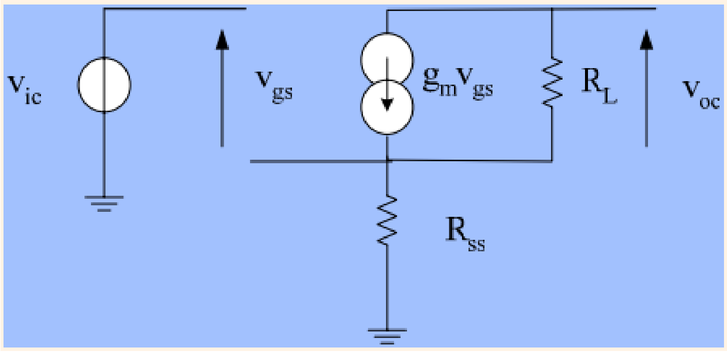


Fig.II.12

Voltage $v_{i2} = 0 \Rightarrow$ M2 grid is connected to ground $\Rightarrow v_{i1} = v_{ic}$
Impossible to neglect the parallel resistance of the current source Rss.

common mode gain : $$A_{cc} = \frac{V_{oc}}{V_{ic}} = -\frac{g_m R_L}{1 + 2g_m R_{SS}} \qquad \text{(II.74)}$$

large Rss resistance, common mode gain is low.

Common mode rejection ratio: $$TRMC = 20\log_{10}\left(1 + 2g_m R_{SS}\right) \qquad \text{(II.75)}$$

II.5 Operational amplifier

Two-stage MOS operational amplifier :

This two-stage diagram contains the following 3 circuits:

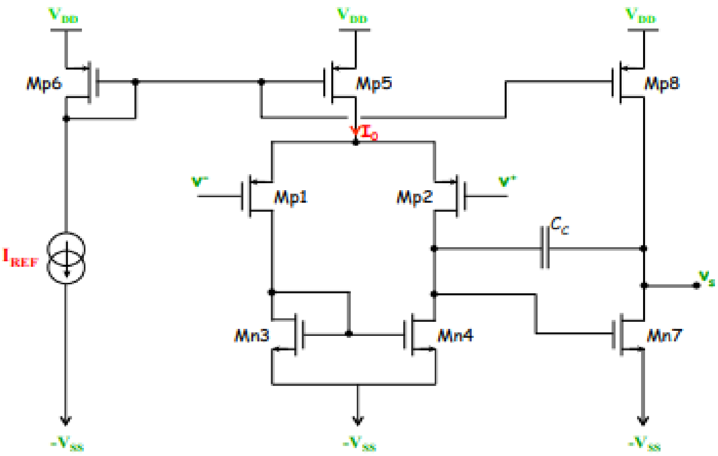


Fig.II.13

- **1st stage: Differential input pair**

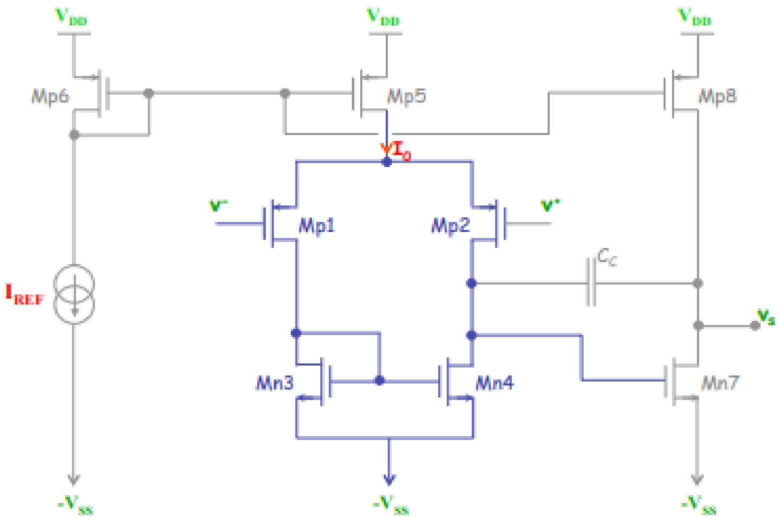


Fig.II.14

- **2nd stage: common source amplifier**

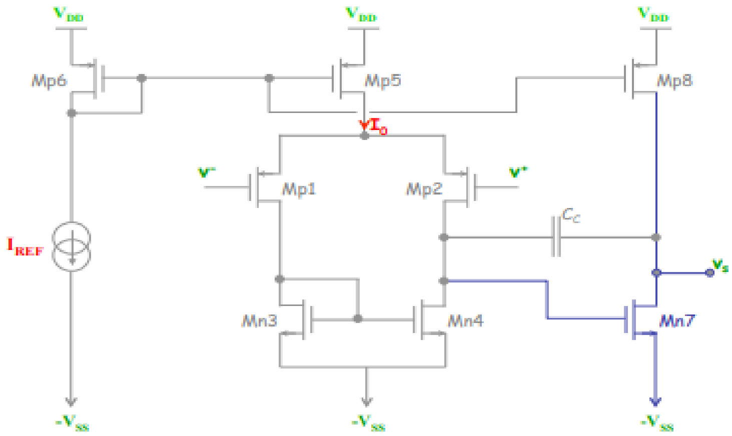


Fig.II.15

- **Polarization**

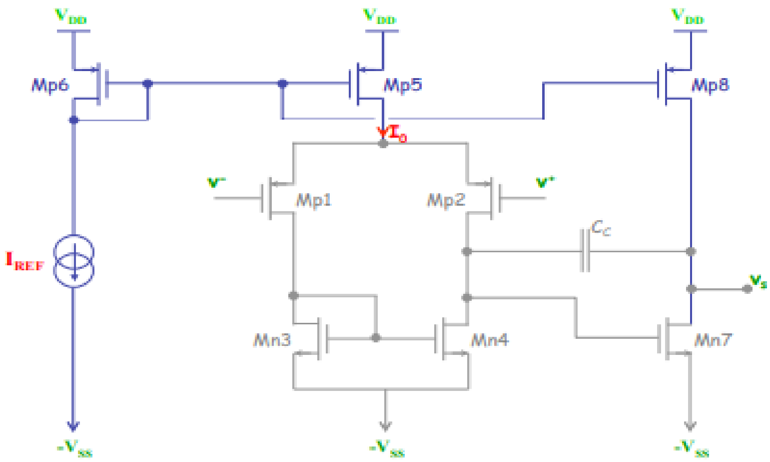
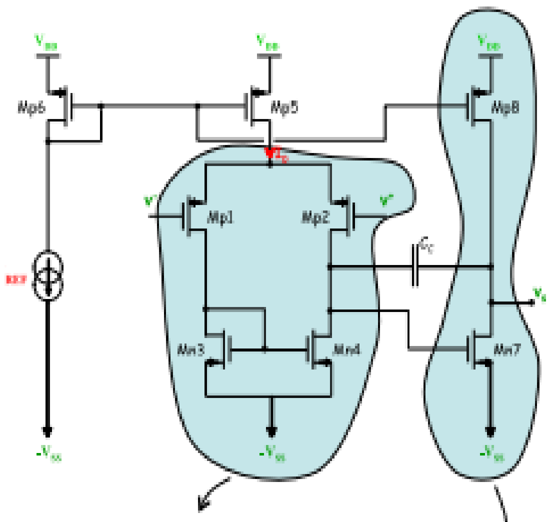


Fig.II.16



$$Z_{in} \approx \infty$$

$$Z_{out} \approx (r_{07} // r_{08})$$

$$A_1 = -g_{m12}(r_{02} // r_{04})$$

Fig.II.17

II.6 Exercises

Exercise 1: (Current Mirror)

The diagram below shows the simplest current source structure in MOS technology. The NMOS transistors; Mn1 and Mn2 are assumed to be saturated. The general form of the drain current is:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{w}{L}(V_{GS} - V_T)^2(1 + \lambda_n V_{DS})$$

1- We will consider Channel Length Modulation (λ = 0): ideal case.

a) Express I_{D1} and I_{D2} the drain currents of Mn1 and Mn2 respectively.

b) Establish a relationship between I_0 (I_{D2}) and I_{REF} (I_{D1}). When do we speak of a current mirror or a current source?

c) Design a current source capable of giving a reference current I_{REF} = 120µA,

Kn = $\frac{1}{2}\mu_n C_{ox}$ = 15 µA.V^{-2} , I_0 (charging current)= 120µA, V_T = 1V, V_{GS2} = 2V.

2- We will consider the Channel Length Modulation (λ ≠ 0) real case.

a) Establish the relationship between I_0 and I_{REF}.

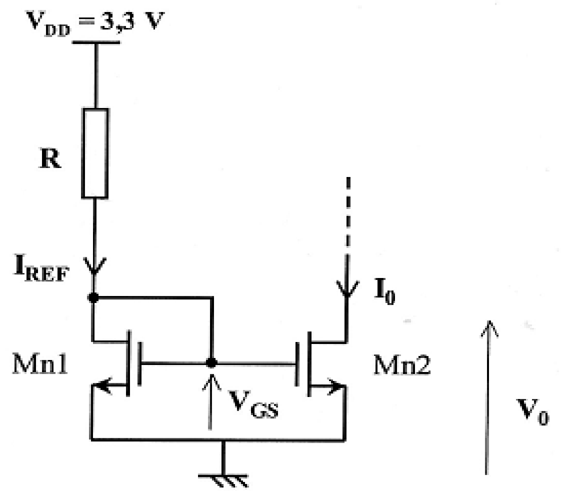
b) What is the value of this relationship between I_0 and I_{REF} in the case where Mn1 and Mn2 are identical?

c) What is the condition for the current source I0 to be stable (considering: λVDS1 << 1).

d) What should be the output resistance r0 of the current source, if I_{REF} = 120µA and λ =1/V_A = 0.015 V^{-1}.

• The metal lines can pass through both the diffusion and the polySi without any electrical effect.

• It is recommended to leave λ between a metal edge and a polySi or diffusion line to which it is not electrically connected.



Solution 1:

1- We will consider Channel Length Modulation (λ = 0): ideal case.

a- $I_{D1} = I_{REF} = k_{n1}(V_{GS} - V_T)^2 \,(1)$

$I_{D12} = I_0 = k_{n2}(V_{GS} - V_T)^2 \,(2) \qquad , V_{GS1} = V_{GS2} = V_{GS}$

b- of (1) et (2) , $I_0 = k_{n2}\dfrac{I_{REF}}{k_{n1}} \Rightarrow I_0 = \dfrac{(W/L)_2}{(W/L)_1} I_{REF}$

We speak of a current mirror or current source if :

$k_{n1} = k_{n2} \Leftrightarrow (W/L)_1 = (W/L)_2 \Rightarrow I_0 = I_{REF}$

c- Design of the current source:

- For Mn2 transistor

We have : $I_0 = \dfrac{1}{2}\mu_n C_{ox}(W/L)_2 (V_{GS2} - V_T)^2 \Rightarrow (W/L)_2 = \dfrac{I_0}{\frac{1}{2}\mu_n C_{ox}(V_{GS2} - V_T)^2}$

$$(W/L)_2 = \frac{120(\mu A)}{15(\mu A/V^2)\times(2-1)(V^2)} = 8 \Rightarrow W_2 = 8L_2$$

- For Mn1 transistor

$$I_{REF} = \frac{1}{2}\mu_n C_{ox}(W/L)_1 (V_{GS1} - V_T)^2 \Rightarrow (W/L)_1 = \frac{I_{REF}}{\frac{1}{2}\mu_n C_{ox}(V_{GS1} - V_T)^2}$$

$$(W/L)_1 = \frac{120(\mu A)}{15(\mu A/V^2)\times(2-1)(V^2)} = 8 \Rightarrow W_1 = 8L_1$$

2- We will consider the Channel Length Modulation (λ ≠ 0) real case.

II.4.4.2 Layout of a CMOS Inverter in Microwind

a- In this case :

$$I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(W/L\right)_1 \left(V_{GS} - V_T\right)^2 \left(1+\lambda V_{DS1}\right)$$

$$I_0 = \frac{1}{2}\mu_n C_{ox}\left(W/L\right)_2 \left(V_{GS} - V_T\right)^2 \left(1+\lambda V_{DS2}\right)$$

Then : $\frac{I_0}{I_{REF}} = \frac{k_{n2}\left(1+\lambda V_{DS2}\right)}{k_{n1}\left(1+\lambda V_{DS1}\right)} \Rightarrow I_0 = I_{REF}\cdot\frac{k_{n2}\left(1+\lambda V_{DS2}\right)}{k_{n1}\left(1+\lambda V_{DS1}\right)}$

b- If Mn1 and Mn2 are identical , $\Rightarrow k_{n1} = k_{n2} \Rightarrow I_0 = I_{REF}\frac{\left(1+\lambda V_{DS2}\right)}{\left(1+\lambda V_{DS1}\right)}$

c- For I_0 (current source) to be stable: It is necessary that: $\frac{dI_0}{dV_{DS2}} = \frac{dI_0}{dV_0}$ tends towards 0.

That is, the output resistance r_0 of the current source is large.

We have : $\lambda V_{DS1} \ll 1 \Rightarrow \frac{dI_0}{dV_{DS2}} \simeq \lambda I_{REF} = \frac{I_{REF}}{V_A} = \frac{1}{r_0} \Rightarrow r_0 = \frac{V_A}{I_{REF}}$

So for : $\frac{dI_0}{dV_{DS2}} \to 0 \Rightarrow r_0$: must be higher

d- If I_{REF} = 120μA, $\lambda = (1/V_A) = 0.015(V^{-1})$,$1/r_0 = I_{REF}/V_A = \lambda I_{REF} = 0.015(V^{-1})$x120 μA, **$r_0$ = 0.5MΩ**

Exercuse 2 :

(a) $V_{GS} = \left(\frac{R_2}{R_1+R_2}\right)V_{DD} = \left(\frac{320}{520+320}\right)(5) = 1.905 \text{ V}$

$I_{DQ} = 0.20(1.905-0.8)^2 = 0.244 \text{ mA}$

$g_m = 2\sqrt{K_n I_{DQ}} = 2\sqrt{(0.2)(0.244)} = 0.442 \text{ mA/V}$

$r_o = \infty$

(b) $A_v = -g_m R_D = -(0.422)(10) = -4.22$

(c) $R_i = R_1 \| R_2 = 520 \| 320 = 198 \text{ K}$

(d) $R_O = R_D = 10 \text{ K}$

Conclusion

This chapter illustrates the power of MOS transistors in analog design. It reinforces the understanding of fundamental principles and acts as a bridge to more complex architectures, while developing the engineer's intuition for circuit analysis.

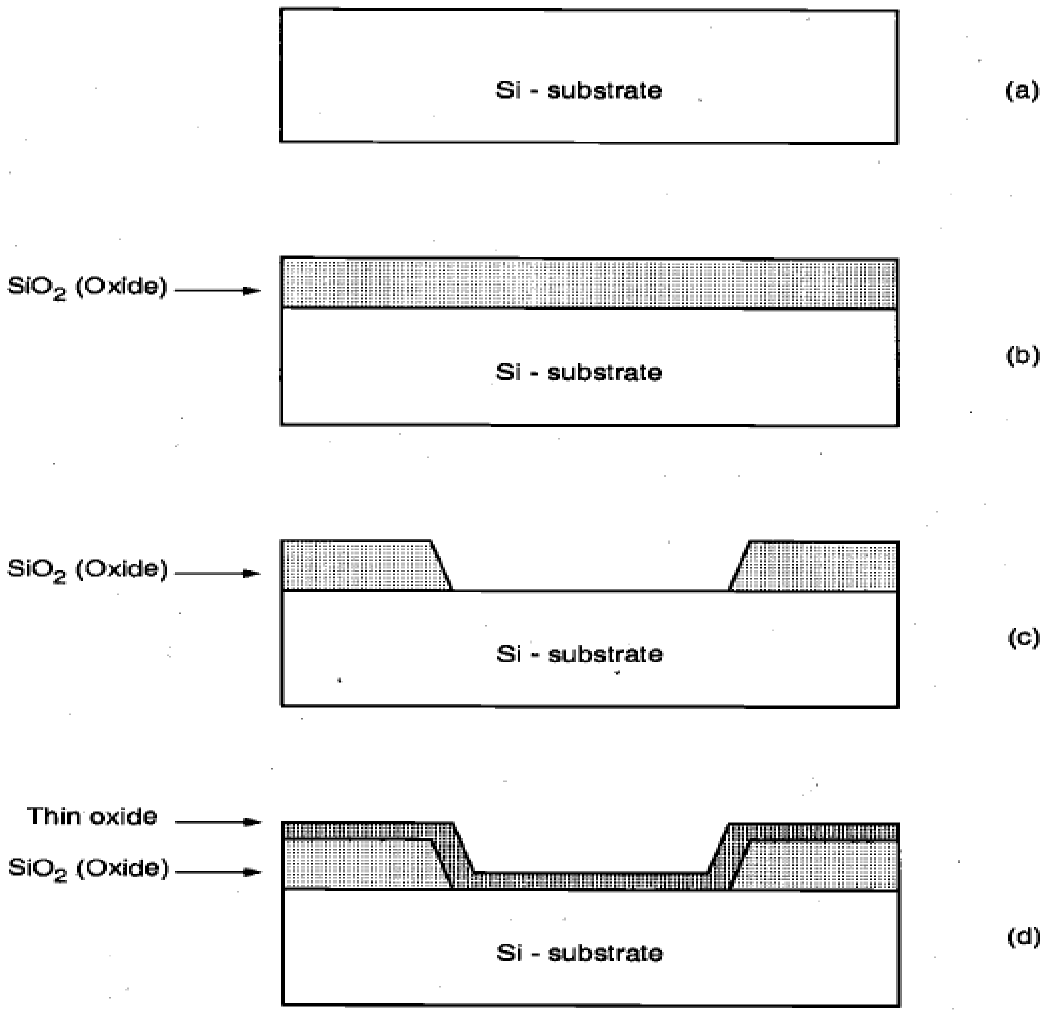
Chapitre III : Mask technology and design (Layout)

Introduction

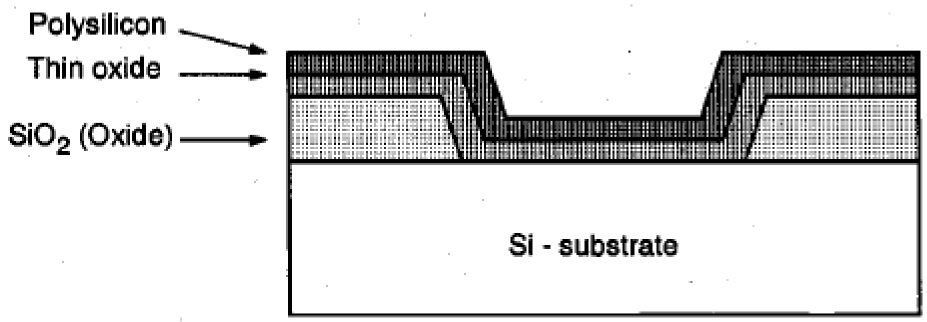
This chapter introduces the manufacturing processes in MOS technology, design rules, mask symbolization, and layout techniques for basic components (resistors, transistors) and analog circuits. It connects the electrical schematic to the physical reality of the chip.

III.1 Manufacturing process using MOS technology

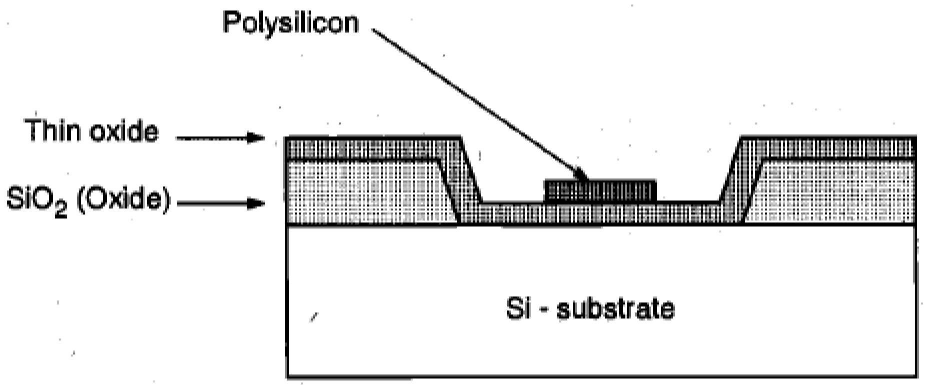
The process starts with the oxidation of silicon substrate (figure a) in which a relative thick silicon dioxide layer also called as field oxide is created on the surface (figure b). Then, the field oxide is selectively etched to expose the silicon surface on which the MOS transistor will be created (figure c). Following this step, the surface is covered with a thin, high-quality oxide layer, which will eventually form the gate oxide of the MOS transistor (figure d).



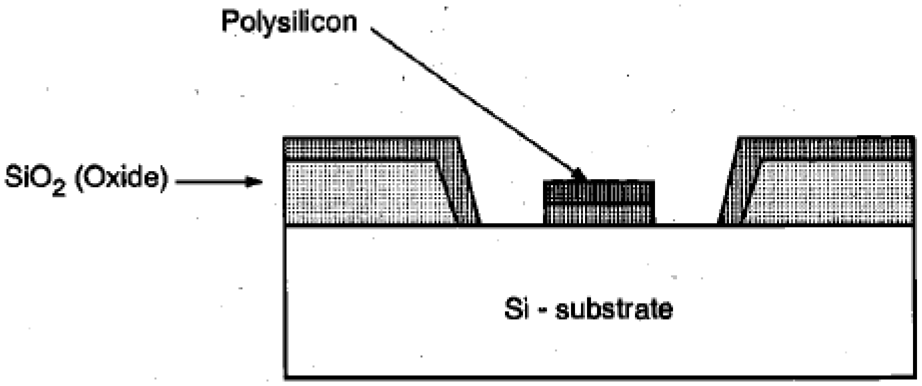
On top of the thin oxide layer, a layer of polysilicon (polycrystalline silicon) is deposited (figure e). After deposition, the polysilicon layer is patterned and etched to form the interconnects and the MOS transistor gates (figure f). The thin gate oxide not covered by polysilicon is also etched away, which exposes the bare silicon surface on which the source and drain junctions are to be formed (figure g).



(e)

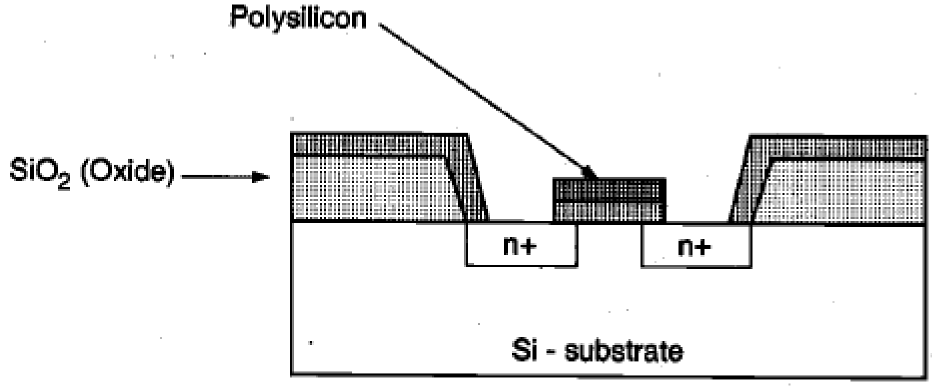


(f)

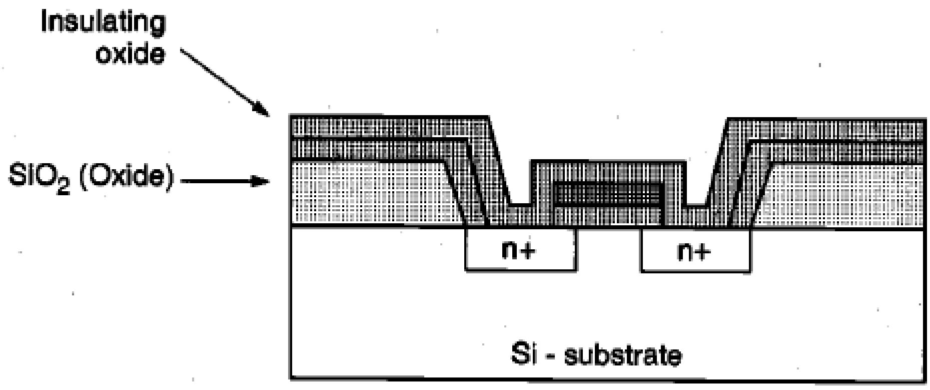


(g)

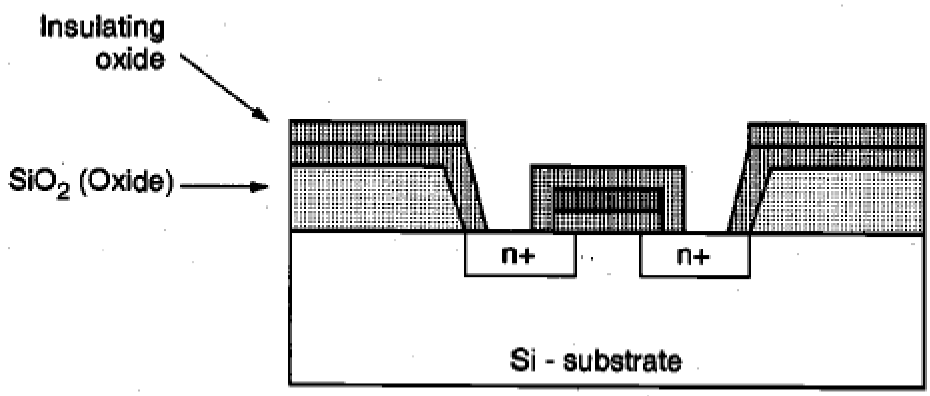
The entire silicon surface is then doped with a high concentration of impurities, either through diffusion or ion implantation (in this case with donor atoms to produce n-type doping). (Figure h) shows that the doping penetrates the exposed areas on the silicon surface, ultimately creating two ntype regions (source and drain junctions) in the p-type substrate. The impurity doping also penetrates the polysilicon on the surface, reducing its resistivity. Once the source and drain regions are completed, the entire surface is again covered with an insulating layer of silicon dioxide (figure i). The insulating oxide layer is then patterned in order to provide contact windows for the drain and source junctions (figure j).



(h)

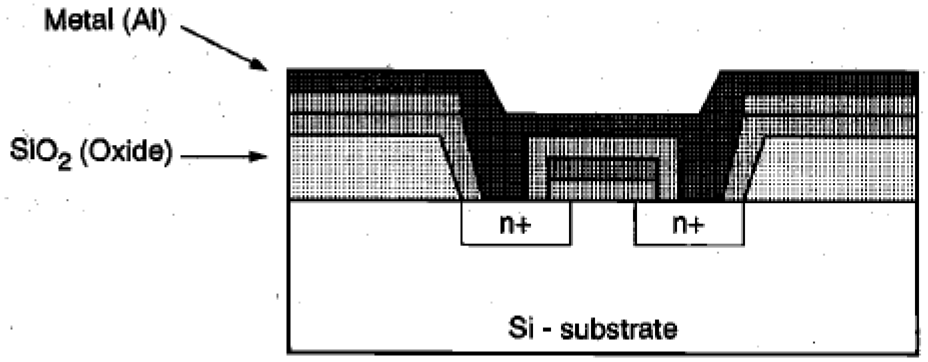


(i)

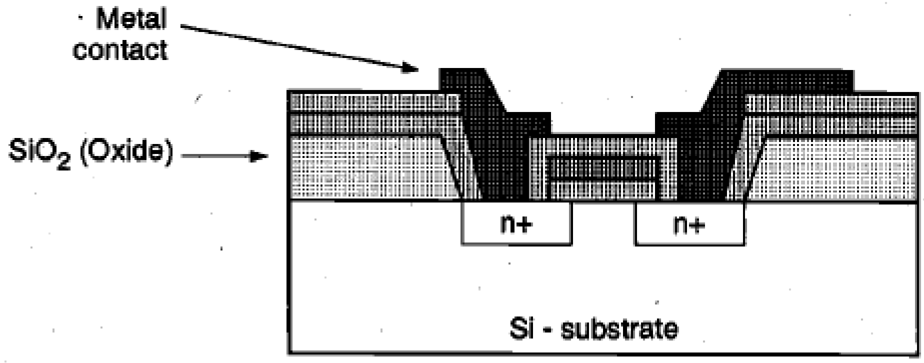


(j)

The surface is covered with evaporated aluminum which will form the interconnects (fig. k). Finally, the metal layer is patterned and etched, completing the interconnection of the MOS transistors on the surface (fig. i).



(k)



(l)

Mask Layout Diagram:-

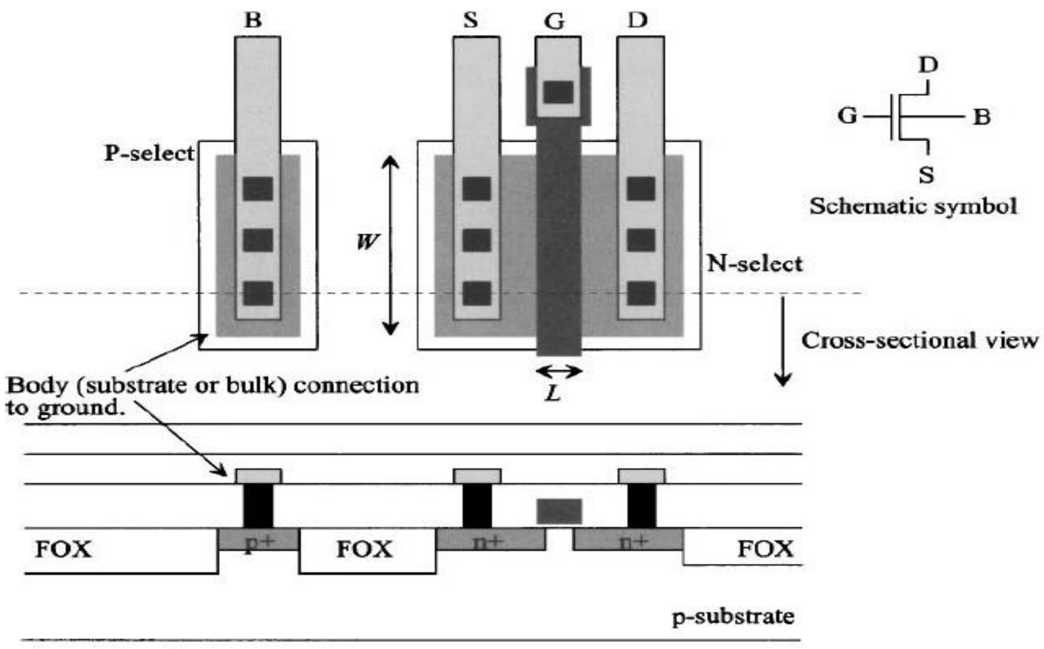


Fig. III.1 The steps of the NMOS transistor manufacturing process

III.2 Drawing rules

1 Mask drawings (Layout)

Layout is a step in the integrated circuit design cycle. In this step, the representation of each component in the circuit is converted into a geometric representation. This representation is actually a set of geometric models that perform the intended function of the corresponding component. The connections between the various components are also expressed as geometric models. The exact details of a layout depend on design rules, which are guidelines based on the limitations of the manufacturing process and the electrical properties of the manufacturing materials.➢ Un circuit numérique est constitué principalement de transistors reliés par des fils conducteurs gravés sur un substrat.

➢ All elements must respect positioning rules (size, distance, overlap, density, etc.)

➢ Each technology (process) imposes its own rules.

Example : – Techno ES2 1µm » 90 rules
– Techno ST 90nm » 400 rules

➢ A new process is created every 18 months.

➢ Circuit design is a very delicate activity and everyone tries to preserve the result so as not to have to redo everything each time.

List of levels : The founder (manufacturer) expects a series of masks (from the designer) allowing the creation of each layer:

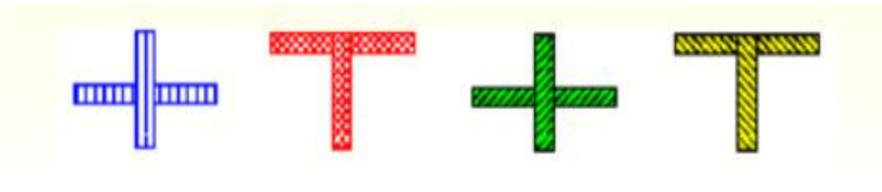
- N-well (possibly P-well)
- active zone
- polysilicon
- N-implantation
- P-implantation
- metal1 cuts (holes from metal1 to wells, polysilicon, or implantations)
- metal1
- metal2 cuts
  metal2, same as metals 3, 4, 5, 6, etc.
- passivation

➡ A total of about twenty layers.

2. Ratings :

layer	color stick notation	color code
n-diffusion		Green
p-diffusion		yellow
polysilicon		red
metal-1		blue
metal-2		dark blue or purple
contact cut		black
via		black
demarcation line		brown
Buried Contact		green

Rule 1: When the same material (on the same layer) touches or crosses each other, they are connected and belong to the same electrical node.

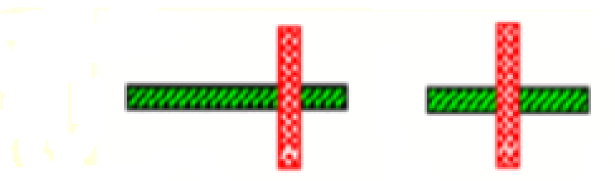


Rule 2 : When polysilicon passes through N or P diffusion, an N or P transistor is formed.

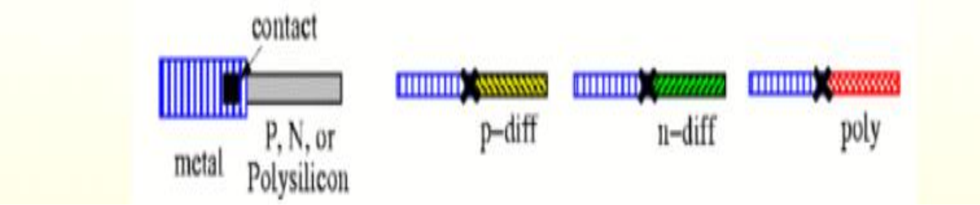
- The polysilicon is drawn above the diffusion.

- Diffusion must be achieved by connecting the source and drain.

- The gate is automatically self-aligned during fabrication.



Rule 3 : When a metallic line is to be connected to one of the other three conductors, a contact break (via) is required.



Rule 4 : In CMOS, a dividing line is drawn to avoid touching p-diff with ndiff. All pMOS must be on one side of the line and all nMOS must be on the other side.

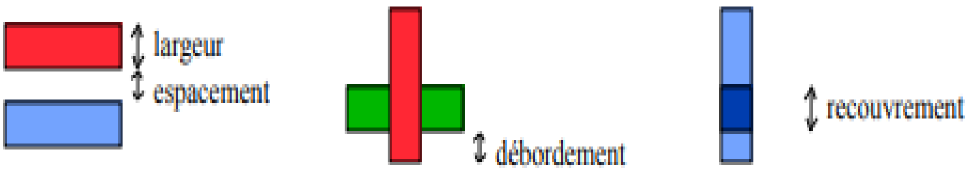
3. Mask drawing rules (layout)

The mask layout stage is the longest and most tedious phase of integrated circuit design. To ensure proper operation, a number of technological rules regarding the dimensions and spacing of these patterns must be respected. The mask design must be done in such a way as to ensure that the drawn structures function correctly after manufacturing. To achieve this, there are a number of constraints to respect during the design: the drawing rules. These rules are highly dependent on the manufacturing process and vary from one manufacturer to another.

3.1 Drawing Rules (DRC)

To verify that the layout is error-free, we use DRC (Design Rule Checking) programs. There are four types:

- **Width :** minimum width allowed for each layer
- **Spacing :** minimum separation between unconnected areas
- **Overflow** : minimum overlap of one layer beyond another
- **Overlap :** minimum overlap distance between two layers



Design rules? Interface between the designer and the founder

In VLSI design, as the process becomes more and more complex, the need for the designer to understand the manufacturing process and interpret the relationships between the different photolithographic masks is really troublesome. Therefore, a set of layout rules, also called design rules, has been defined. They serve as an interface or communication link between the circuit designer (Designer) and the process engineer (Founder) during the manufacturing phase. The objective associated with the layout rules is to obtain a circuit with optimal efficiency (functional circuit versus non-functional circuits) in the smallest possible area without compromising the reliability of the circuit.

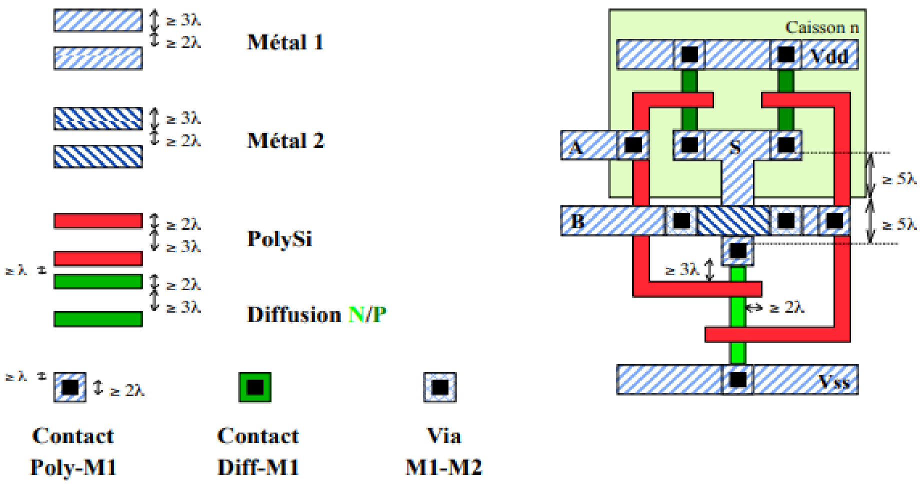
Two major approaches :

– Rules « Micron » : All minimum sizes and spacings specified in microns.

– Rules « Lambda » : All minimum sizes and spacings specified in lambda parameters.

4. Lambda-Based Design Rules λ

- Rules for an example process



- Drawing of a MOS transistor

A layout of a MOS transistor is identified by memorizing the following rule: each intersection between the polysilicon (POLY1) and diffusion (DIFF) layers corresponds to a MOS transistor (fig II.41).

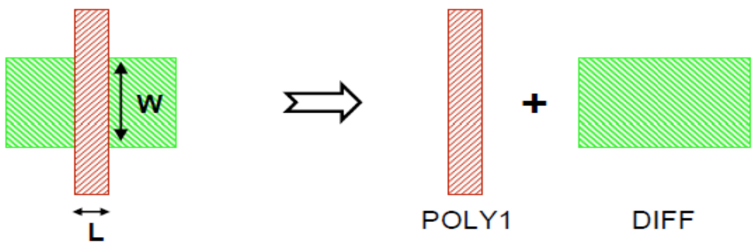


Fig.III.2 Definition of a MOS transistor.

The grid length (L for length) and the grid width (W for width) are read directly on the layout and correspond to those of the POLY1 - DIFF intersection.

5. Example: some design rules for 1.2µm technology

(default technology in Microwind) **Layout design rules**.

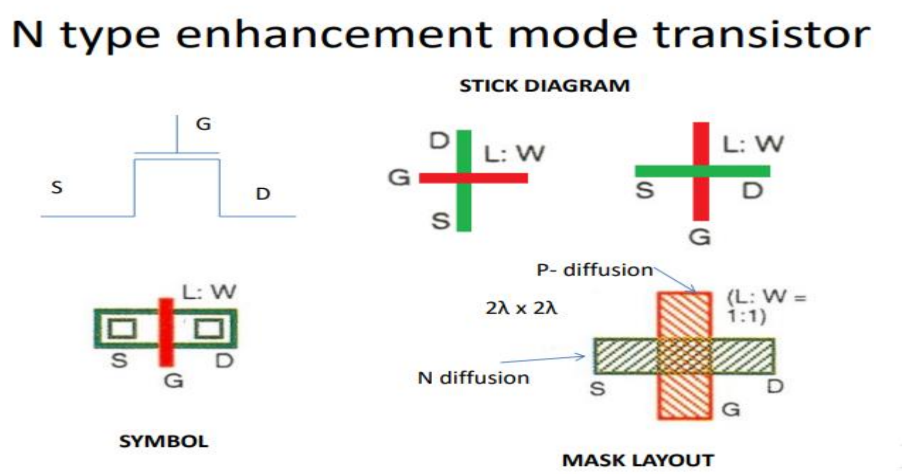
- The operation of the MICROWIND software is based on a lambda grid, not a micro grid.
- The value of lambda λ is half of the minimum gate length L in polysilicon. λ = L/2. Table II.1 gives the correspondence between lambda and micron for all CMOS technologies supported by Microwind (simulation software for mask design).

Table III.1 Correspondence between technology and the value of lambda λ in µm

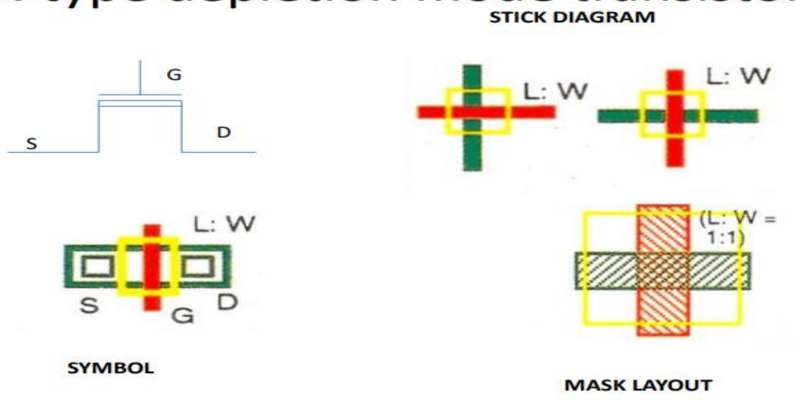
Technology	Minimum grid length	The value of lambda
Cmos12.rul	1.2 µm	0.6 µm
Cmos08.rul	0.7 µm	0.35 µm
Cmos06.rul	0.5 µm	0.25 µm
Cmos035.rul	0.4 µm	0.2 µm
Cmos025.rul	0.25 µm	0.125 µm
Cmos018.rul	0.2 µm	0.1 µm
Cmos012.rul	0.12 µm	0.06 µm
Cmos90n.rul	0.1 µm	0.05 µm
Cmos65n.rul	0.07 µm	0.035 µm
Cmos45n.rul	0.05 µm	0.025 µm

III.3 Symbolic drawing

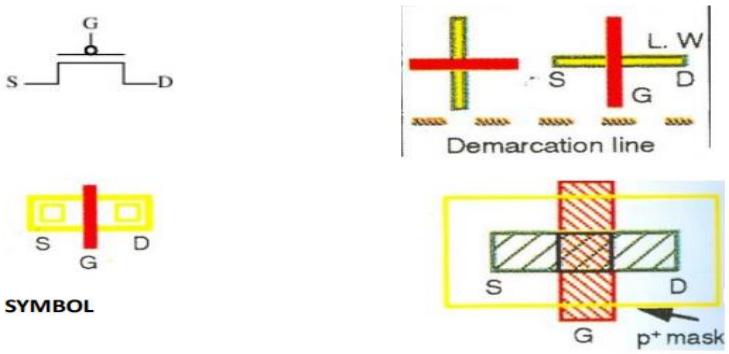
We first laid out an NMOS transistor and then a PMOS transistor. Then combining these (CMOS) we constructed an inverter gate.



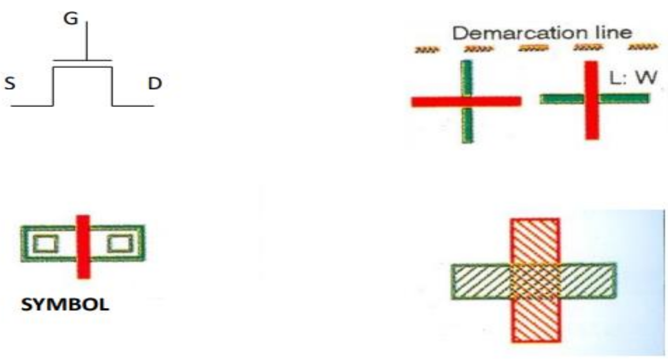
N type depletion mode transistor



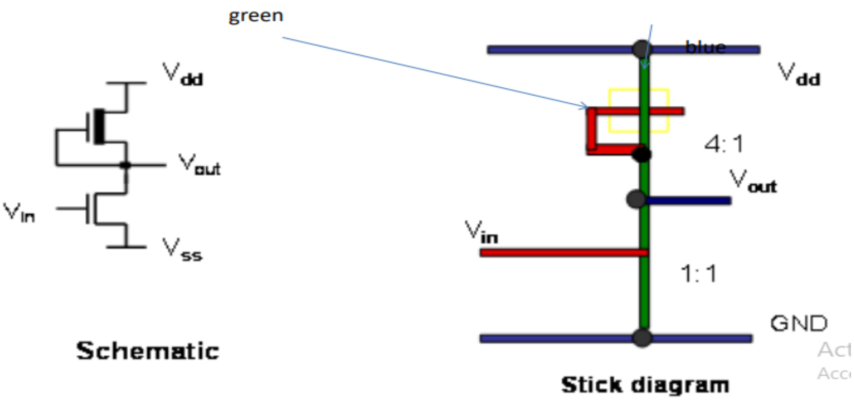
P type enhancement mode transistor in cmos p-well process



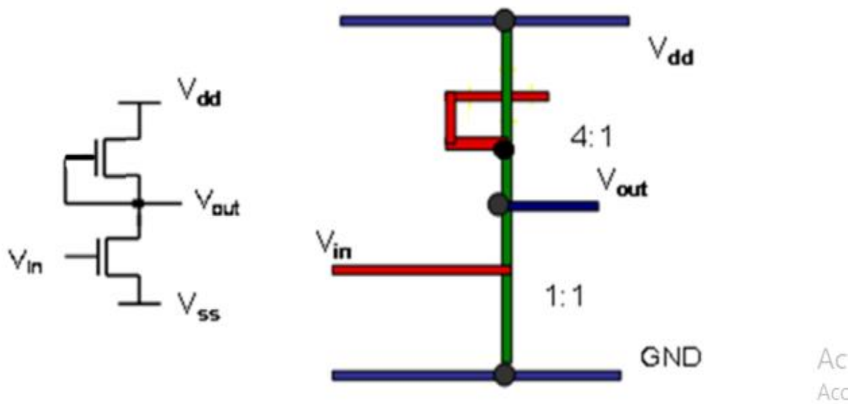
N type enhancement mode transistor in cmos p-well process



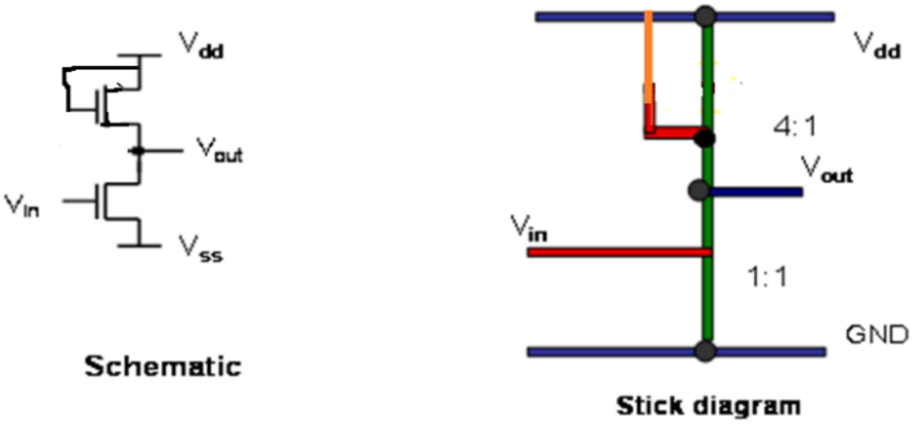
nMOS depletion load inverter

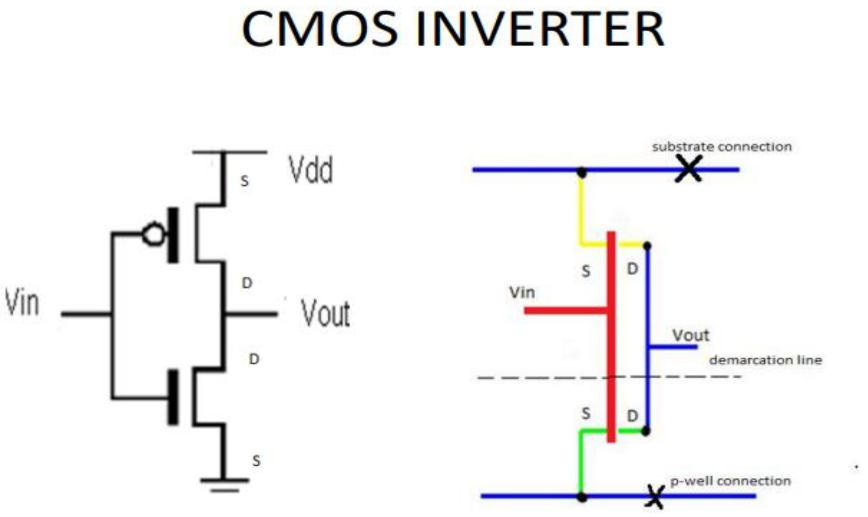


nMOS enhancement load inverter



nMOS enhancement load inverter





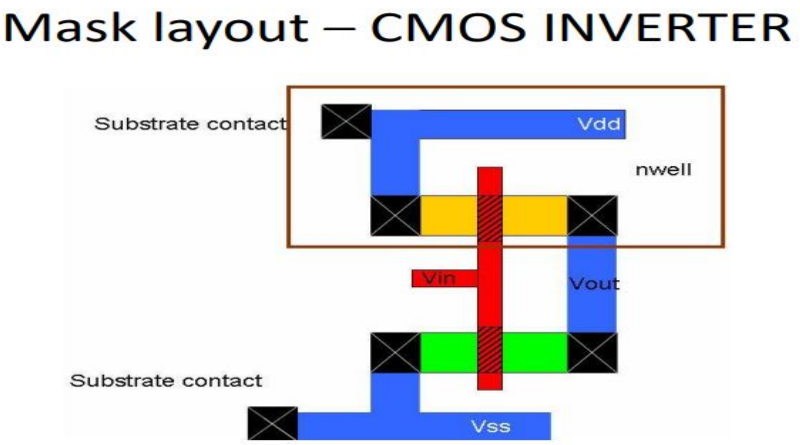


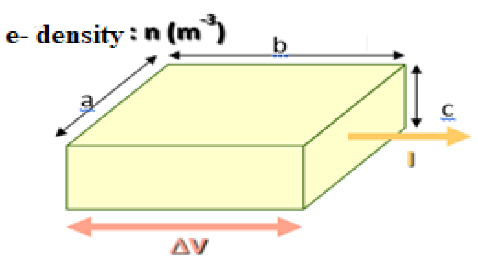
Fig.III.3 Symbolic drawing for MOS Transistor

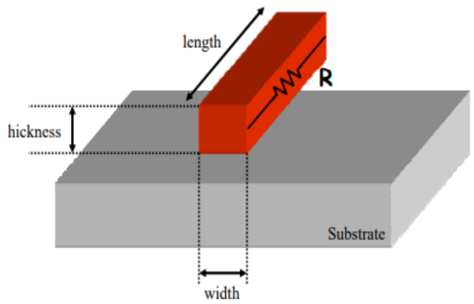
III.4 Mask drawing of a resistor and a MOS transistor

III.4.1 Mask drawing of a resistor

The principle is to create, in a given level, a strip long enough to obtain the desired value.

- **Resistivity of a material** :





$$R = \rho \cdot \frac{l}{w \cdot t} \Rightarrow R = \frac{\rho}{t} \cdot \frac{l}{w} \Rightarrow R = R \cdot \frac{l}{w}$$

Fig.III.4 Sheet Resistor

- ✓ Elementary volume charge : $|Q| = nqabc$
- ✓ Speed of e- (assumed uniform) : $|V_d| = \mu|E| = \mu\frac{\Delta V}{b}$, μ : is a mobility
- ✓ Transit time of an e- through the volume : $\tau = \frac{b}{|V_d|}$
- ✓ Resulting current : $I = \frac{|Q|}{\tau} = \frac{nqabc}{\tau} = nqac|V_d| = nqac\mu\frac{\Delta V}{b}$
- ✓ Ohm's Law : $I = G\Delta V$

We therefore find a conductance of the form : $G = \sigma\frac{ac}{b}$ with $\sigma = nq\mu$, material conductivity

The resistance is therefore worth : $R = \frac{\rho}{c}\frac{b}{a}$ with $\rho = 1/\sigma$ (resistivity) : then, $$\mathbf{R = R_{/\square}\,\frac{b}{a}}$$

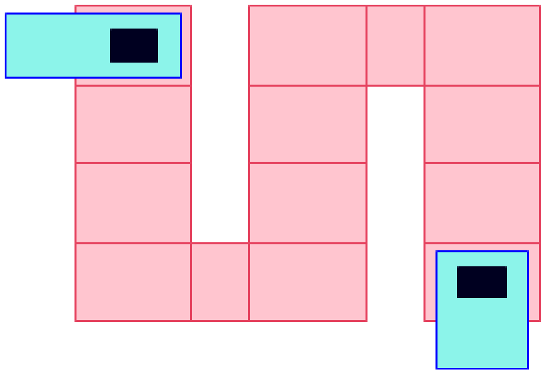
(III.1)

- **Drawing of a resistor**

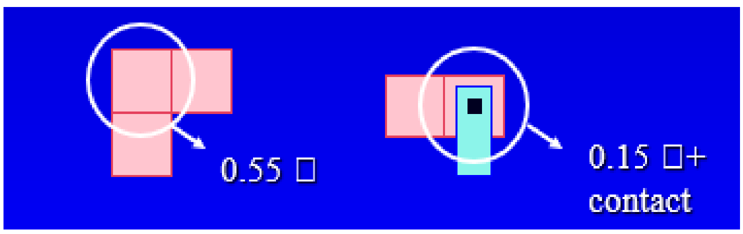
There are two types of built-in resistors :

<u>Polysilicon</u> **$R_{/\square}$ = qq 10 W**

n- well **$R_{/\square}$ = qq 1kW (but more significant nonlinear effects)**



Coils are generally made to save space.

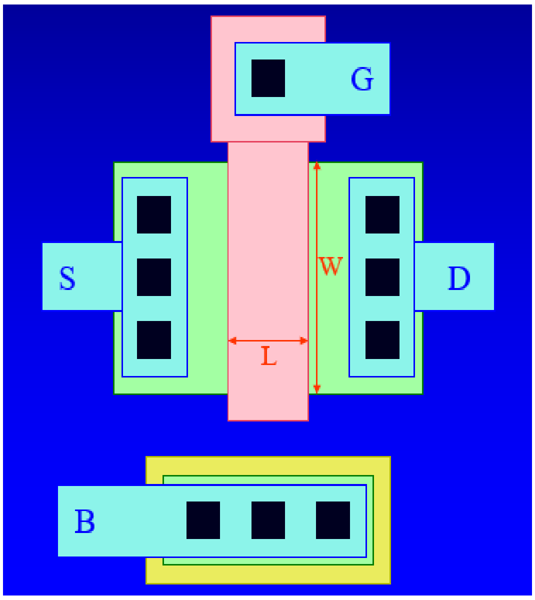


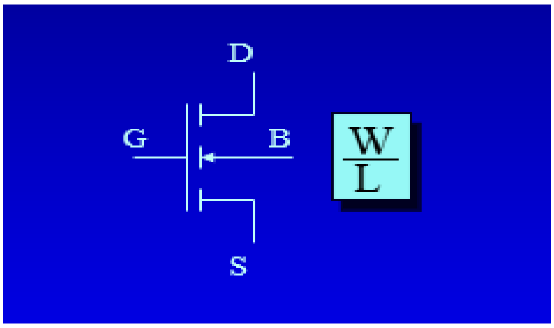
<u>Exemple :</u>

R = 7 * R/• + 4 * 0.55 * R/• + 2 * 0.15 * R/• + 2 * Rcnt

The integrated resistors are temperature-dependent because μ varies with T.

III.4.2 Mask drawing of a MOS transistor





The effective size of the transistor is much larger than the useful area (W*L).

The layout introduces parasitic .elements: additional capacitors and resistors

From the designer's perspective, we will operate with three representations of MOS circuits as shown in Figure 4.8.

These three representations are:

• Schematic diagrams.

• Stick diagrams representing the integrated circuit topology.

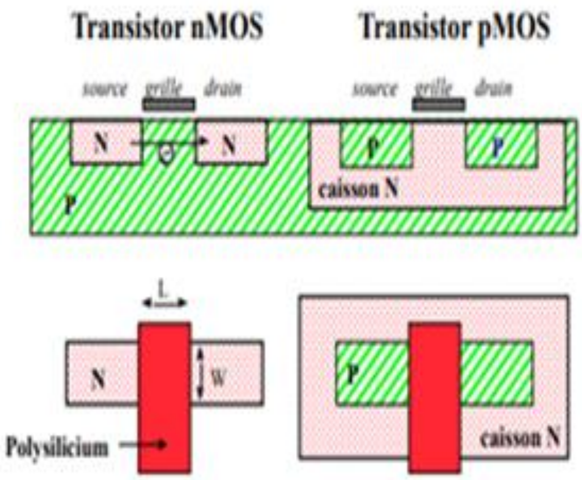
• Circuit layout representing the exact geometry of the integrated circuit.

The circuit geometry must have its dimensions specified in relative units called λ.

X nm or 2λ technology

λ : smallest mask design size

Canal transistor :2λ



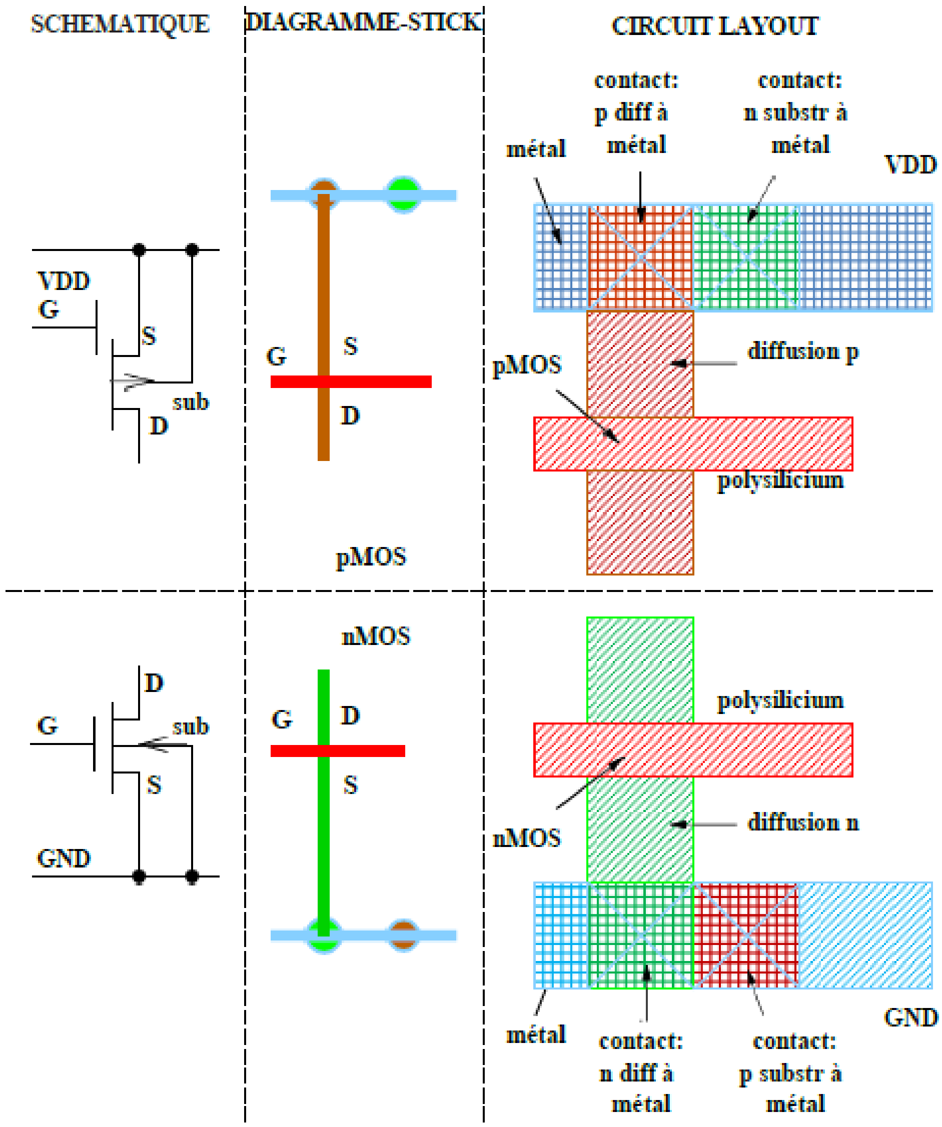
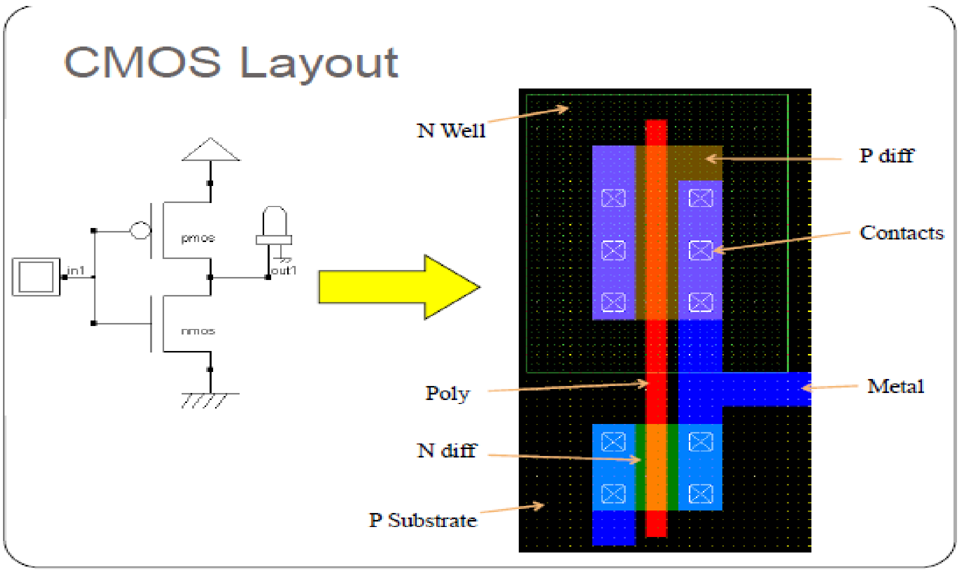


Fig. 4.8 les Trois représentations de la circuiterie MOS : schémas, diagramme et layout.

III.5 Mask drawing of an analog circuit



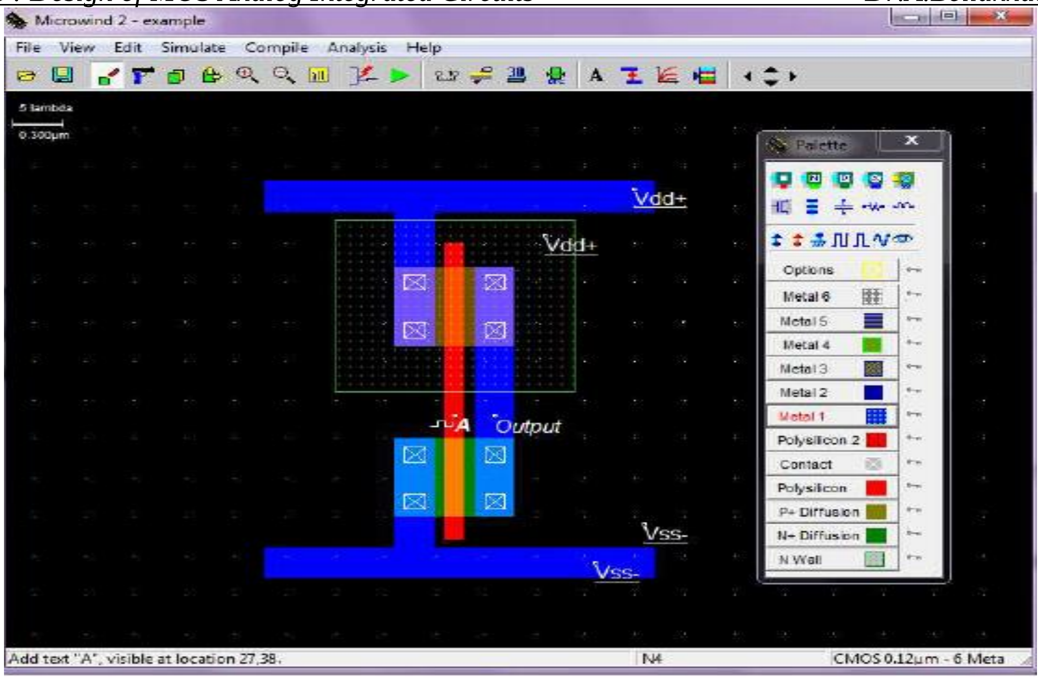


Figure II.42 Layout de l'inverseur CMOS dans Microwind

III.6 Questions and Exercises:

1- Questions :

1- Define the Lambda design rules used for layout ?
2- What is the need for design rules?
3- Define any two layout design rules.

Answers :

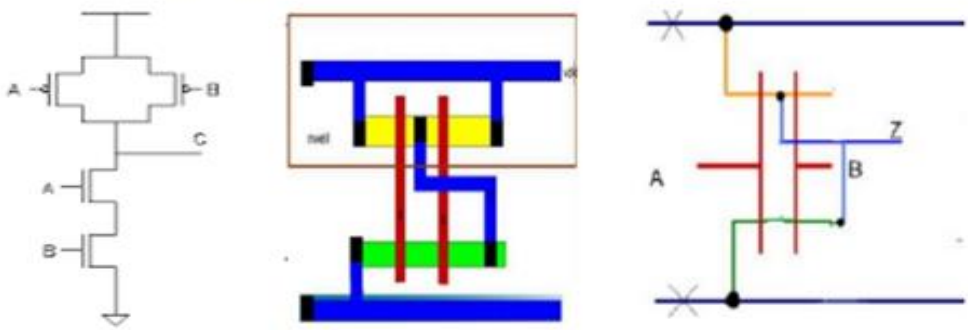
1- Lambda rule specify the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of a single parameter (λ) and thus allow linear, proportional scaling of all geometrical constraints.
2- Design rules are the communication link between the designer specifying requirements and the fabricator who materializes them. Design rules are used to produce workable mask layouts from which the various layers in silicon will be formed or patterned.
3- **Micron design rule:**
Micron rules specify the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of absolute dimensions in micrometers.
Lambda design rule:

Lambda rule specify the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of a single parameter (λ) and thus allow linear, proportional scaling of all geometrical constraints.

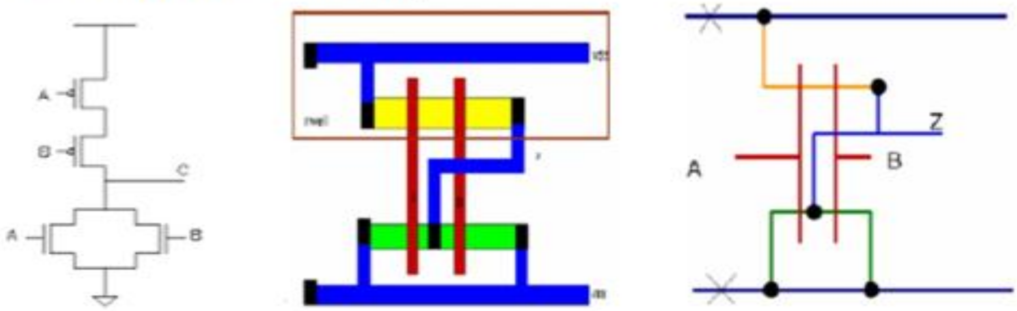
Exercice : Draw the layout diagram for NAND and NOR gate for CMOS inverter.

Answer :

- **Layout diagram for NAND gate:**



- **Layout diagram for NOR gate:**



Conclusion

This section is crucial for transitioning from logical design to the physical implementation of the circuit. Mastery of layout directly impacts performance, reliability, and silicon area. The chapter emphasizes strict adherence to design rules and provides a foundation for using CAD tools.

General Conclusion

This handout offers a comprehensive and structured training on MOS transistor design and their use in analog circuits. Starting from the physical and technological fundamentals, it gradually guides the student toward mastering modeling, simulation, circuit analysis, and physical design. Each chapter builds a key skill and prepares the reader to face the challenges of modern microelectronics. With the integration of practical examples, exercises, and simulation methods, this material is an effective educational tool for students in electronics and integrated circuit design.

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