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Theme

Phase-Locked Loop Design for Grid-Connected Converters under unbalanced grid Conditions

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Abstract

The purpose of this master project is to investigate different phase locked loop (PLLs) architectures for grid-voltage synchronization under different kinds of grid conditions such as frequency and magnitude variations. After introducing PLL basics, we presented different convention PLL methods used for grid-synchronization (single as well as three phase systems). For the case of three phase systems, we investigated the difference between the following methods: i) abc-frame PLL, ii) $\alpha\beta$-PLL and, iii) dq-frame PLL, and how one can design the controller parameters. Despite the fact that these methods work well under frequency and amplitude variations of the grid voltages, they are sensible to phase shift disturbances and distorted signals. The last part of this report is dedicated to an advanced PLL structure, known as decoupled double synchronous reference frame PLL (DDSRF-PLL). Simulation results show that the PLL in question guarantee better performance compared to conventional methods with respect to phase shift variations.

Keywords: PLL, Phase locked loop, *abc*-frame PLL, $\alpha\beta$-frame PLL, *dq*-frame PLL, DDSRF PLL.

Contents

List of Figures

General Introduction

Power electronic converters are essential elements to inject generated energy by renewable energy power systems to the power grid. Besides the challenging problem of controlling these converters, it is required to get an information about the phase angle of the grid voltages for synchronization purposes. This is achieved using PLLs, a shortened form of Phase Locked Loops.

Phase locked loops concept dates back to 1919 where Vincent and Appleton studied the practical synchronization of oscillators [1, 2]. They are widely used in many applications such as: modulation and demodulation of signals, frequency synthesizer in telecommunication systems, clock generation and much more. A PLL is a feedback system with three main elements: i) phase detector, ii) loop filter and iii) an oscillator. It allows to track the phase angle of a periodic signal and its angular velocity.

For safe synchronization of inverter outputs with the grid voltages, we need a PLL in order to track continuously, the phase angle (fundamental angular frequency) of the grid voltage. The most used conventional PLL methods for grid synchronization are:

- abc-frame PLL,
- $\alpha\beta$-PLL and,
- dq-frame PLL.

These methods are efficient and commonly used under balanced grid voltages, but in case of unbalanced scenarios these do not give accurate results [2].

In this project, we will investigate the performance of four different PLL techniques: three conventional methods and a Decoupled Double Synchronous Reference Frame PLL (DDSRF-PLL) under normal and abnormal grid voltage conditions. This thesis is divided on three chapters besides the introduction and the conclusion:

- **In chapter one**, we will present the phase locked loop, its structure and how it works and and its applications in different fields.

- **The second chapter** is devoted to the grid synchronization techniques for single and three phase systems.

- **The third chapter** is dedicated to the presentation of the decoupled double synchronous reference frame PLL and different simulation results. All methods are tested and compared under four grid voltage conditions: 1) a set of three-phase balanced voltages, 2) a set of three-phase unbalanced voltages in magnitudes and 3) a set of three-phase unbalanced voltages in phase shift.

Chapter 1

Phase Locked Loop – Generalities

1.1 Introduction

This chapter will discuss Phase-Locked Loop basics and terms, its applications in multiple fields, and its advantages and disadvantages, but first, we will start with a brief history of PLLs.

1.2 Basic Structure of a Phase Locked Loop

Phase-locked loop structures may be considered relatively new for most of us, but historical literature dates the concept as early as 1919 where Vincent and Appleton experimented and analyzed, respectively, the practical synchronization of oscillators [1]. After this initial paper, research and development continued up until the 1940s where the initial interest in synchronization was for a) a local oscillator in FM demodulation and b) the exciter for an atomic particle accelerator amplifier [2, 3]. The control theory for phase-locked loops was based on the well-developed theory for feedback amplifiers.

A Phase-Locked Loop circuit is simply a control feedback system that adjusts its state to match the phase of an input signal. The basic structure of a PLL is shown in Fig. 1.1. It has three common blocks as highlighted in the introduction [4]:

- A phase detector;
- A low pass filter;

- A voltage controlled oscillator (VCO).

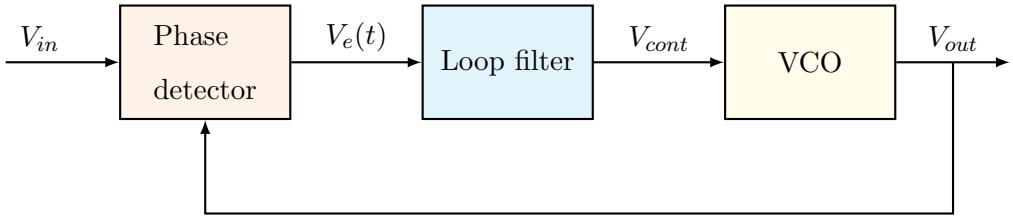


Figure 1.1: Basic structure of a PLL.

The voltage-controlled oscillator produces a periodic signal V_{out}, and the phase detector compares its phase with the phase of an input periodic signal V_{in}, and through a loop filter, the oscillator is adjusted to keep the phases of both signals ($\Phi_{in}(t)$ and $\Phi_{out}(t)$) matched.

1.2.1 Phase Detector:

It compares the phase at each input and generates an error signal, $V_e(t)$, proportional to the phase difference between the two inputs.

As an example, one can use an analog multiplier as a phase detector. Consider the following two signals $A(t)$ and $B(t)$ given by:

$$A(t) = a\cos(\omega_1 t + \phi_A)$$
$$B(t) = b\cos(\omega_2 t + \phi_B)$$

Then:

$$V_e(t) = A(t)B(t) = \frac{ab}{2}\left(\cos((\omega_1 + \omega_2)t + \phi_A + \phi_B) + \cos(\phi_A - \phi_B)\right)$$

Since the two inputs are at the same frequency when the loop is locked ($\omega_1 = \omega_2$), we have one output at twice the input frequency and an output proportional to the cosine of the phase difference.

1.2.2 Loop Filter:

The periodic signal with doubled frequency component must be removed by the low pass loop filter. The design of the PLL loop filter is crucial to the operation of the whole phase locked loop. The actual circuit of the PLL loop filter is generally remarkably simple, but it has a major impact on the performance of the loop.

1.2.3 Voltage Controlled Oscillator (VCO)

The signal with phase difference ($\cos(\phi_A - \phi_B)$ in the previous example) shows up as the control voltage to the VCO, a DC or slowly varying AC signal after filtering. Then, the VCO generates a signal whose frequency varies with respect to a central frequency as a function of the input voltage.

1.3 PLL properties

1.3.1 Lock In Range

Range of input signal frequencies over which the loop remains locked once it has captured the input signal. This can be limited either by the phase detector or the VCO frequency range.

1.3.2 Capture Range

When the PLL is initially not in lock, what frequency range can make PLL lock is called as capture range. This is also known as acquisition range. This is directly proportional to the LPF bandwidth. Reduction in the loop filter bandwidth thus improves the rejection of the out of band signals, at the same time the capture range decreases, pull in time becomes larger and phase margin becomes poor.

1.3.3 Pull In Time

The total time taken by the PLL to capture the signal (or to establish the lock) is called as Pull in Time of PLL. It is also called as Acquisition Time of PLL.

1.3.4 Bandwidth Of PLL

Bandwidth is the frequency at which the PLL begins to lose the lock with reference.

1.4 Applications of PLL

PLL circuit is used in wide range applications in the area of electronics, communication and instrumentation. Some of PLL applications are highlighted in the next subsections.

1.4.1 Modulation and Demodulation

When analog signals are modulating a high frequency carrier the PLL is needed to demodulate the received signal back to the baseband. Classical modulation scheme include amplitude modulation (AM) ,frequency modulation (FM) and phase modulation (PM). An important application was found in 1950, the color subcarrier in Televisions systems was recovered with the use of a PLL.

1.4.2 Frequency Synthesis

The important application of PLL in the field of frequency synthesis is creating a signal with correct and stable frequency, it is commonly found in the sending part of the communication systems where the carrier is created for bandpass signaling. By synthesis we mean that a signal from an oscillator is fed to the PLL and the output is a signal with another frequency.

Frequency synthesizer can produce a large number of frequency sources which have the same accuracy and stability as the high precision and high stability reference frequency input. After the process of frequency mixing, frequency multiplication and frequency division, the reference frequency can be made full use of by the frequency synthesizer.

The method of frequency synthesis using phase locked loop is called indirect synthesis, which is the most widely used method of frequency synthesis. The most commonly used circuits are phase-locked frequency multiplication circuit and phase-locked frequency division circuit.

Phase-locked frequency multiplication circuit (there is a frequency divider in the feedback branch) is shown below Fig. 1.2:

$$\omega_0 = N\omega_i \tag{1.1}$$

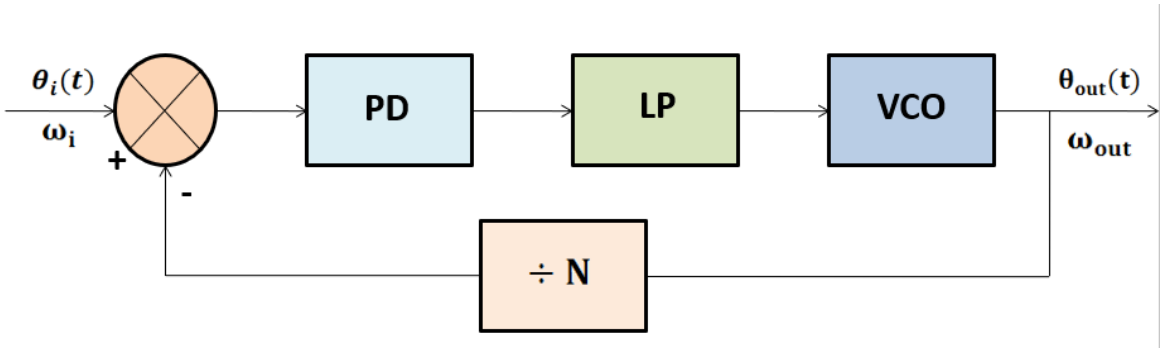


Figure 1.2: Phased-locked frequency multiplication schematic diagram.

Phase-locked frequency division circuit can be obtained by considering frequency multiplier in the feedback branch.

1.4.3 Clock Generation

Many electronic systems include processors of various sorts that operate at hundreds of megahertz. Typically, the clocks supplied to these processors come from clock generator PLLs, which multiply a lower-frequency reference clock (usually 50 or 100 MHz) up to the operating frequency of the processor. The multiplication factor can be quite large in cases where the operating frequency is multiple GHz and the reference crystal is just tens or hundreds of megahertz.

1.4.4 Carrier Recovery (Clock Recovery)

Some data streams, especially high-speed serial data streams (such as the raw stream of data from the magnetic head of a disk drive), are sent without an accompanying clock. The receiver generates a clock from an approximate frequency reference, and then phase-aligns to the transitions in the data stream with a PLL. This process is referred to as clock recovery.

1.4.5 Skew Reduction

This is one of the very popular and earliest uses of PLL. Suppose synchronous pair of data and clock lines enter a large digital chip. Since clock typically drives a large number of transistors and logic interconnects, it is first applied to large buffer. Thus, the clock distributed on chip may suffer from substantial skew with respect to data. This is an undesirable effect which reduces the timing budget for on-chip operations.

1.4.6 Jitter and Noise Reduction

One desirable property of all PLLs is that the reference and feedback clock edges be brought into very close alignment. The average difference in time between the phases of the two signals when the PLL has achieved lock is called the static phase offset. The variance between these phases is called tracking jitter. Ideally, the static phase offset should be zero, and the tracking jitter should be as low as possible.

1.5 PLL Advantages And Disadvantages

PLLs have several advantages and disadvantages we will start with the advantages :

1.5.1 Advantages Of PLL

The advantage of phase-lock loops is that they receive an input signal, compare this to the feedback of their internal clock generated by a voltage-controlled oscillator (VCO), and adjust the VCO by way of the charge pump to match the new input frequency and synchronize the internal and external clocks.

It has many advantages such as high reliability, stability, and easy adjustment, short transmission delay, less occupation of hardware resources, reliable phase discrimination, design flexibility, easy to modify and achieve, power management and noise sensitivity.

It is a great advantage for a designer of high-performance systems to use a PLL-based clock driver.

1.5.2 Disadvantages of PLL

Then we have the disadvantages that make their use in high-speed designs problematic, particularly when both high performance and high reliability are required.

We have also the PLL voltage-controlled oscillator (VCO) it is the greatest source of problems. Variations in temperature, supply voltage, and manufacturing process affect the stability and operating performance of PLLs.

1.6 Conclusion

After the study that has been done in this chapter we learned about the Phase Locked Loop Structure in general, how it works, this allows us to introduce the application of PLL in grid which is the aim of the next chapter " PLL Application in Grid-Connected Converters".

Chapter 2

PLL Application in Grid-Connected Converters

2.1 Introduction

In this chapter, we will present different grid synchronization techniques for *single phase systems* as well as *three phase systems*. For the single phase system, we will concentrate on two methods: i) a PLL method based on T/4 delay and ii) a PLL method based on inverse park transformation. For three phase system, we will present three conventional methods:

- abc Reference Frame PLL.
- Stationary Reference Frame PLL ($\alpha\beta$-PLL).
- Synchronous Reference Frame PLL (dq-PLL).

Then, we will present the difference between these methods in a rigourous manner.

2.2 Basic control of Grid-connected Power Converter

Figure 2.1 shows grid-connected power converters in a distributed generation system. These converters can be affected by various grid faults because of many factors. The control of these power converters under abnormal condition should guarantee that the

protection of the converter would not trip but also need to support the grid voltage under these conditions.

Grid faults mostly give rise of unbalanced grid voltages and as a result the currents injected into the grid get non-sinusoidal and lose their balanced operation. As a result the combination of these unbalanced grid voltages and such currents give rise to uncontrolled oscillations in the active and reactive power delivered to the network. The accurate operation of the power converter under these conditions is one of the main control task [5].

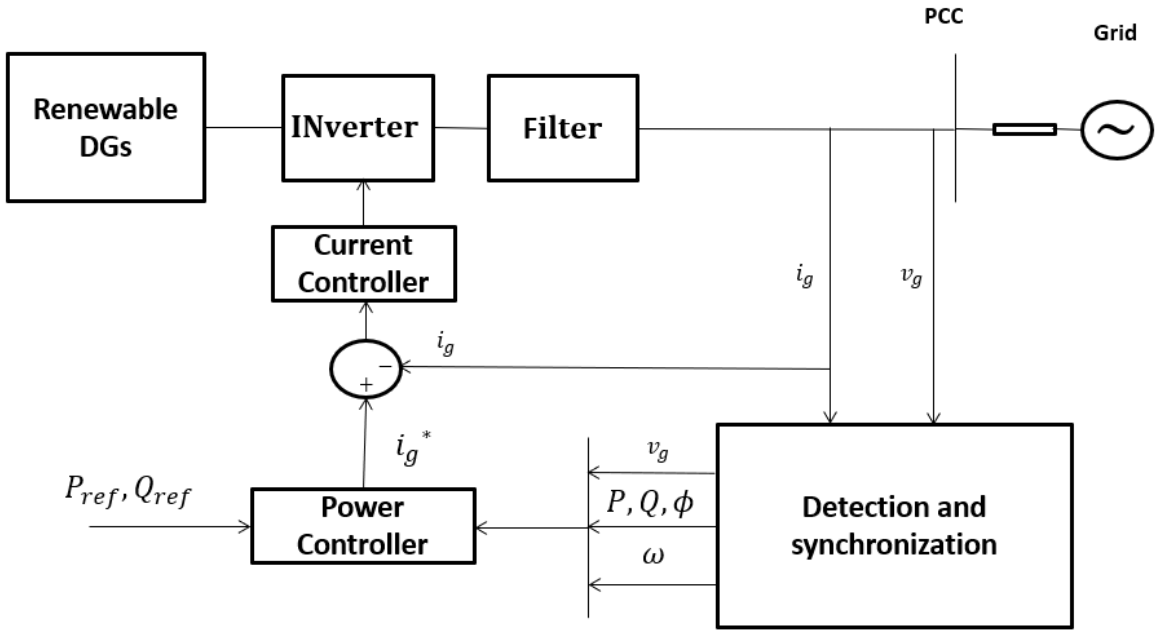


Figure 2.1: Grid tied renewable DG systems with its control Structure.

Grid-voltage synchronization algorithm has the ability to detect the phase angle of the grid voltages which is used to generate references for the converter controller. In the sequel, we will show different schemes of phase locked loop used in single phase systems as well as three phase systems.

2.3 PLL for single phase grid synchronization

Grid synchronization of single-phase grid-connected converters lies in the accurate detection of the attributes of the grid voltage in order to tune an internal oscillator of the power converter controller to the oscillatory dynamics imposed by the grid.

Usually, the main attributes of interest for interfacing renewable energies to the grid by using power converters are the **amplitude** and the **phase-angle** of the fundamental frequency component of the grid voltage.

The time-domain detection methods are based on some kind of adaptive loop that enables an internal oscillator to track the component of interest of the input signal. The most extended synchronization method in engineering applications, the phase-locked loop (PLL).

Figure 2.2 illustrates a basic PLL structure for single phase systems. The application of a simple PLL structure for synchronizing with the low-frequency voltage of a conventional grid (50/60 Hz) will provide evidence of the need to improve its structure by using some kind of quadrature signal generator.

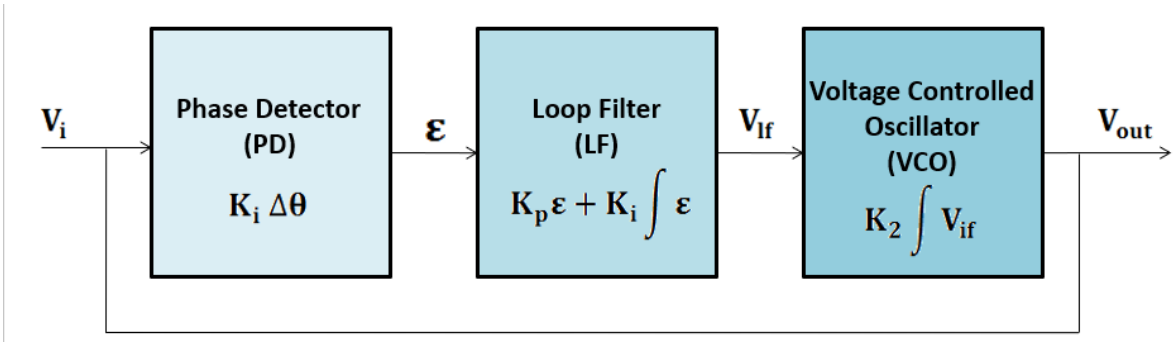


Figure 2.2: Basic PLL structure for single phase

For most of the single-phase grid tied power conditioning systems, such as active power filters, dynamic voltage restores, flexible AC transmission systems (FACTs), uninterrupted power supplies (UPS), the most vital required information to connect with grid are *phase-angle* and *frequency* of the utility grid. And to estimate these phase-angle and frequency of single-phase signals, various methods have been proposed in previous studies.

Accurate knowledge of phase and frequency of grid voltage under these conditions is hard to obtain but crucial for converter operation and control. Various grid synchronization schemes have been reported to address the grid requirements and comparative studies of some of them have been carried out and published in [6, 7, 8]. Here the phase difference between the input and output signal is measured by the phase detector (PD), then it is passed through a loop filter (LF), which is a low pass filter. The

voltage controlled oscillator (VCO) is driven by the output signal of the loop filter (LF) to generate the overall output signal, which will follow the input signal [9].

Several PLL methods have been proposed to synchronize power transfer to the grid for single phase systems. In the sequel, we will present the following two methods:

- A PLL method based on T/4 delay.
- A PLL method based on inverse park transformation.

PLL algorithms are derived from the standard structure presented in the previous chapter which has three main parts: phase detector (PD), Loop filter (LF), and Voltage controlled oscillator (VCO).

2.3.1 PLL based on T/4 delay

When the fundamental grid frequency time period is T, using first-in-first-out (FIFO) buffer the $T/4$ transport delay technique can be implemented, by setting its size to one fourth of the number of samples contained in one cycle of the fundamental frequency.

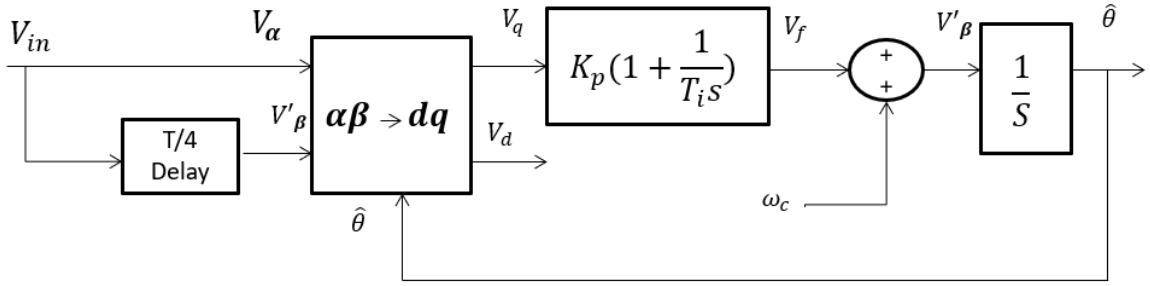


Figure 2.3: Basic T/4 delay based PLL structure

As shown in Fig 2.3, considering an input signal which is the component and creating a component by delaying V_i by $\pi/2$ i.e $T/4$ w.r.t. fundamental frequency of the input voltage. And then transforming these V_α and V_β, from $\alpha\beta$ to dq by using Park's transformation, it can be used in detecting the phase error.

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \begin{bmatrix} V_m \cos\Delta\theta \\ -V_m \sin\Delta\theta \end{bmatrix} \tag{2.1}$$

This technique is a simple one to extract phase-angle in single-phase application. If the input voltage signal is purely sinusoidal waveform at a rated grid frequency then only it works well [6]. Because the orthogonal signal output will not be perfect if the grid frequency changes, and this will rise to errors in synchronization. And also it doesn't have any filtering capability, so if there is any harmonic components in the input voltage, that will disrupt the PLL.

2.3.2 PLL based on Inverse Park's Transform

In this method we will build an orthogonal signal generator, which is supposed to generate the 'β' component, a loop consisting of direct as well as indirect Park's transform supported by two low pass filters is created as shown in Fig. 2.4. But here the condition is the PLL should be perfectly tuned to the input frequency to make V_α to be in phase with V_α and in quadrature with V_β . And also the nonlinear inner loop must be fast enough to generate the 'β' component [10, 11]. The whole technique can be described by these set of equations :

$$V_{dq}(s) = \begin{bmatrix} V_d(s) \\ V_q(s) \end{bmatrix} = T_p \begin{bmatrix} V_{in}(s) \\ V_\beta(s) \end{bmatrix} \tag{2.2}$$

$$V_{\alpha\beta}(s) = \begin{bmatrix} V'_\alpha(s) \\ V'_\beta(s) \end{bmatrix} = T_p^{-1} \begin{bmatrix} V'_d(s) \\ V'_q(s) \end{bmatrix} \tag{2.3}$$

$$\begin{bmatrix} V'_d(s) \\ V'_q(s) \end{bmatrix} = G_L(s) \begin{bmatrix} V_d(s) \\ V_q(s) \end{bmatrix} = \frac{\omega_L}{s + \omega_L} \begin{bmatrix} V_d(s) \\ V_q(s) \end{bmatrix} \tag{2.4}$$

2.4 PLL For Three-Phase Systems Grid Synchronization

The most used conventional PLL methods for grid synchronization in three phase systems are:

- abc-frame PLL,

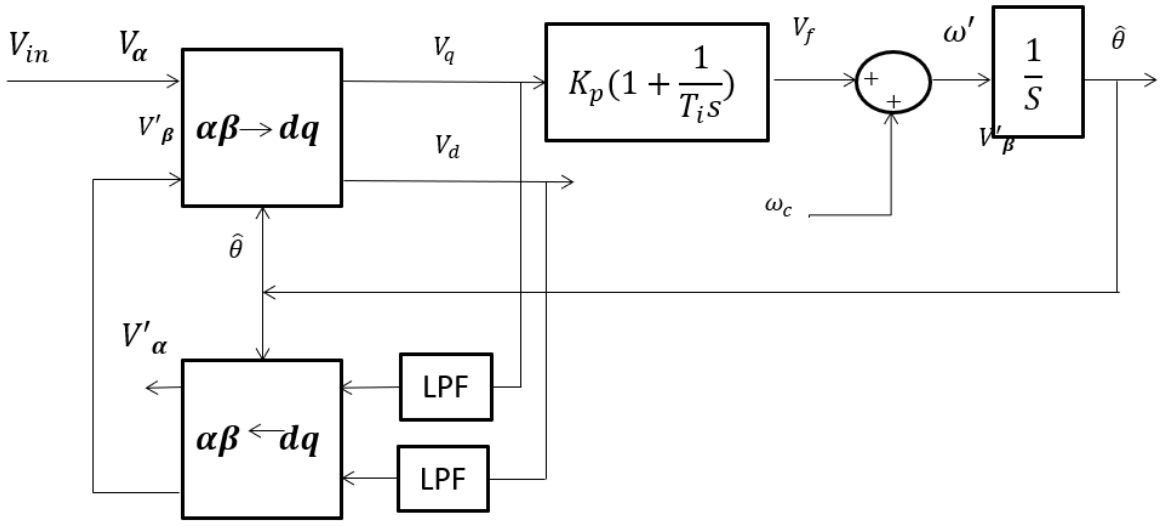


Figure 2.4: PLL based on Inverse Park's Transform

- $\alpha\beta$-PLL and,
- dq-frame PLL.

Let us start by the first method description.

2.4.1 abc Reference Frame PLL (abc-PLL):

The abc-PLL technique determines the fundamental angular frequency and phase angle of grid voltages under balanced grid voltage condition. Fig. 2.5 shows the basic scheme of abc-PLL. This technique is based on the computation of the fictitious instantaneous active power. The expression for fictitious instantaneous active power is:

$$P' = V_a I_a + V_b I_b + V_c I_c$$

2.4.2 Stationary Reference Frame PLL ($\alpha\beta$-PLL):

The $\alpha\beta$-PLL achieves synchronization in the stationary $\alpha\beta$-reference frame that translates the natural abc-reference frame into the stationary $\alpha\beta$-reference frame.

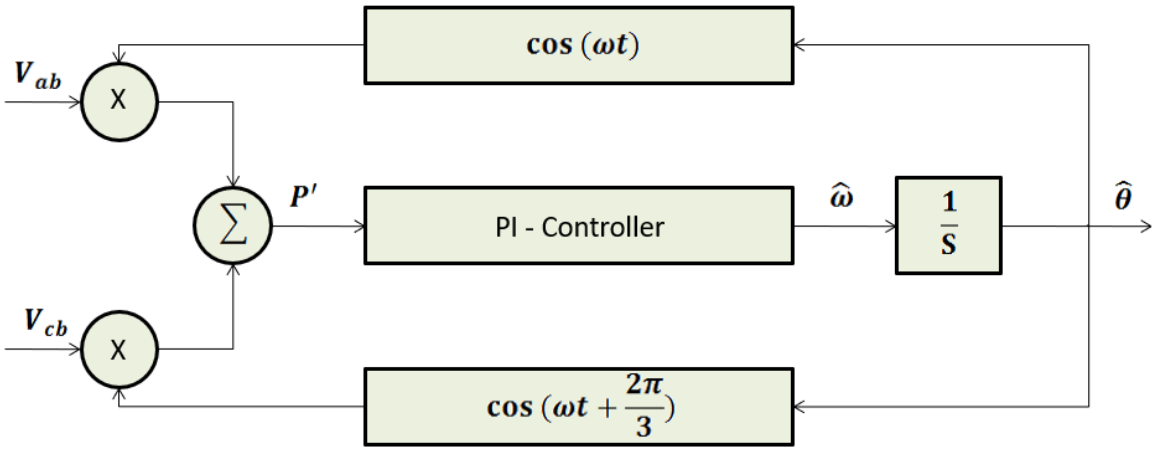


Figure 2.5: Basic Block Diagram Of abc Pll

The structure of the $\alpha\beta$-PLL is shown in Fig. 2.6, which is used to generate the phase error. Thus, controlling it to track a zero reference through a PI controller leads to the extraction of the phase. The $\alpha\beta$-PLL is able to estimate the phase angle for balanced grid conditions. However, it also fails to accurately operate under unbalanced grid faults. The inaccuracies due to the unbalanced sequence can be compensated by reducing the bandwidth of the synchronization control loop. The only advantage of the $\alpha\beta$-PLL contrast to the dq-PLL is that the frequency overshoot at the time of faults is smaller.

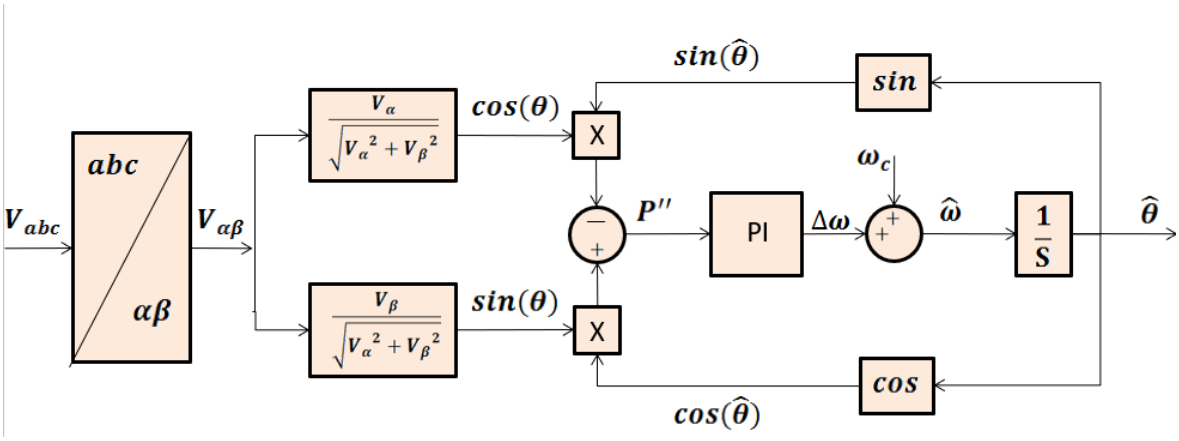


Figure 2.6: Basic Block Diagram Of The $\alpha\beta$-PLL System.

2.4.3 Synchronous Reference Frame PLL (dq-PLL):

The dq-PLL is designed according to the Clarke and Park transformation, shown in (2.5), which converts the natural abc-reference frame into the synchronous dq-reference frame [12]. To acquire the phase of the input voltages, the q-component of the positive sequence voltage in (2.5) tracks a zero reference through a PI controller, the loop filter .

As a result, under ideal voltage conditions, θ dq-PLL equal to the phase angle of the three-phase voltage and component V_d perfectly tracks the magnitude of the positive sequence voltage V_+. Since the synchronous frame is rotating with the positive angular speed, the dq-PLL works accurately for balanced grid faults. It fails to track the phase angle when an unbalanced fault occurs. This is because of the presence of double-line frequency oscillations induced by the negative sequence components V_- that disturb the dq-components resulting in the mismatch of V_d from the positive sequence magnitude $|V_+|$[5]. In addition, the dq-PLL cannot work for harmonically distorted three-phase voltages. The structure of the dq-PLL is presented in Fig. 2.7.

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos(\theta - 120) & \cos(\theta + 120) \\ -\sin\theta & -\sin(\theta - 120) & -\sin(\theta + 120) \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{2.5}$$

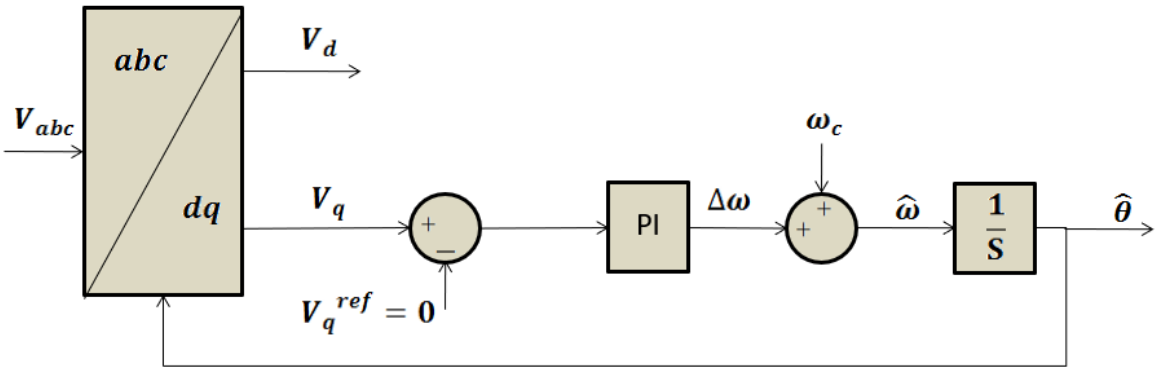


Figure 2.7: Basic bloc diagram of dq-PLL.

2.5 Difference between PLL conventional methods

In this section, we will highlight the difference between conventional methods. Let us start by the first PLL: abc-frame PLL.

2.5.1 abc-frame PLL

From Fig. 2.5, we have:

$$p' = -(V_b - V_a)\cos\hat{\theta} - (V_b - V_c)\cos(\hat{\theta} + \frac{2\pi}{3})$$

$$= \begin{bmatrix}\cos\hat{\theta} & -\cos\hat{\theta} & 0\end{bmatrix}\begin{bmatrix}V_a\\V_b\\V_c\end{bmatrix} + \begin{bmatrix}0 & -\cos(\hat{\theta}+\frac{2\pi}{3}) & \cos(\hat{\theta}+\frac{2\pi}{3})\end{bmatrix}\begin{bmatrix}V_a\\V_b\\V_c\end{bmatrix}$$

$$= \begin{bmatrix}\cos\hat{\theta} & -\cos\hat{\theta} - \cos(\hat{\theta}+\frac{2\pi}{3}) & \cos(\hat{\theta}+\frac{2\pi}{3})\end{bmatrix}\begin{bmatrix}V_a\\V_b\\V_c\end{bmatrix}$$

Hence,

$$p' = \begin{bmatrix}\cos\hat{\theta} & -\cos(\hat{\theta}+\frac{\pi}{3}) & \cos(\hat{\theta}+\frac{2\pi}{3})\end{bmatrix}\begin{bmatrix}V_a\\V_b\\V_c\end{bmatrix}$$

and for a three phase balanced system:

$$V_a = V_{max}\sin(\omega t) \tag{2.6}$$

$$V_b = V_{max}\sin(\omega t - \frac{2\pi}{3}) \tag{2.7}$$

$$V_c = V_{max}\sin(\omega t + \frac{2\pi}{3}) \tag{2.8}$$

we have the following terms:

- **Term 1:**

$$\cos\hat{\theta}V_a = \cos\hat{\theta}\sin\theta \tag{2.9}$$

- **Term 2:**

$$-\cos(\hat{\theta}+\tfrac{\pi}{3})V_b = -\cos(\hat{\theta}+\tfrac{\pi}{3})\sin(\theta-\tfrac{2\pi}{3})$$

$$= -\left(\cos\hat{\theta}\cos(\frac{\pi}{3})-\sin\hat{\theta}\sin(\frac{\pi}{3})\right)\left(\sin\theta\cos(\frac{2\pi}{3})-\cos\theta\sin(\frac{2\pi}{3})\right)$$

$$= \left(\frac{1}{2}\cos\hat{\theta}-\frac{\sqrt{3}}{2}\sin\hat{\theta}\right)\left(\frac{1}{2}\sin\theta+\frac{\sqrt{3}}{2}\cos\theta\right)$$

Thus,

$$-\cos(\hat{\theta}+\frac{\pi}{3})V_b = \frac{1}{4}\cos\hat{\theta}\sin\theta-\frac{3}{4}\sin\hat{\theta}\cos\theta+\frac{\sqrt{3}}{4}\cos\hat{\theta}\cos\theta-\frac{\sqrt{3}}{4}\sin\hat{\theta}\sin\theta \quad (2.10)$$

- **Term 3:** We have,

$$\cos(\hat{\theta}+\tfrac{2\pi}{3})V_c = \cos(\hat{\theta}+\tfrac{2\pi}{3})\sin(\theta+\tfrac{2\pi}{3})$$

$$= \left[\cos\hat{\theta}\cos(\tfrac{2\pi}{3})-\sin\hat{\theta}\sin(\tfrac{2\pi}{3})\right]\left[\sin\theta\cos(\tfrac{2\pi}{3})+\cos\theta\sin(\tfrac{2\pi}{3})\right]$$

$$= \left[-\tfrac{1}{2}\cos\hat{\theta}-\tfrac{\sqrt{3}}{2}\sin\hat{\theta}\right]\left[-\tfrac{1}{2}\sin\theta+\tfrac{\sqrt{3}}{2}\cos\theta\right]$$

Thus, the third term is given by:

$$\cos(\hat{\theta}+\frac{2\pi}{3})V_c = \frac{1}{4}\cos\hat{\theta}sin\theta-\frac{3}{4}\sin\hat{\theta}\cos\theta-\frac{\sqrt{3}}{4}\cos\hat{\theta}\cos\theta+\frac{\sqrt{3}}{4}\sin\hat{\theta}\sin\theta \quad (2.11)$$

From (2.9)-(2.11), the input of the PI controller, $p^{'}$, is given by:

$$p' = \frac{3}{2}\cos\hat{\theta}\sin\theta-\frac{3}{2}\sin\hat{\theta}\cos\theta \Rightarrow P' = \frac{3}{2}\sin(\theta-\hat{\theta}) \quad (2.12)$$

2.5.2 $\alpha\beta$-frame PLL

From the $\alpha\beta$- frame PLL structure shown in Fig. 2.6 and after simplifications, we can easily prove the following:

$$\frac{V_\alpha}{\sqrt{V_\alpha^2 + V_\beta^2}} = \cos\theta \tag{2.13}$$

$$\frac{V_\beta}{\sqrt{V_\alpha^2 + V_\beta^2}} = \sin\theta \tag{2.14}$$

$$V_{max} = \sqrt{V_\alpha^2 + V_\beta^2} \tag{2.15}$$

which yields:

$$p^{''} = \sin(\theta)\cos(\hat{\theta}) - \cos(\theta)\sin(\hat{\theta})$$

Simplifying this equation, the input of the PI controller is given by:

$$p^{''} = V_{max} sin(\theta - \hat{\theta}) \tag{2.16}$$

2.5.3 dq-frame PLL

The transformation of abc voltages to dq-frame is given by the following equations:

$$\begin{bmatrix} V_d \\ V_q \\ V_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \sin\hat{\theta} & \sin(\hat{\theta} - \frac{2\pi}{3}) & \sin(\hat{\theta} + \frac{2\pi}{3}) \\ \cos\hat{\theta} & \cos(\hat{\theta} - \frac{2\pi}{3}) & \cos(\hat{\theta} + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}$$

The V_q component fed to the PI controller corresponds to:

$$V_q = \frac{2}{3}\left[\frac{3}{2} cos\hat{\theta} sin\theta - \frac{3}{2} sin\hat{\theta} cos\theta\right]$$

and a simplified version:

$$V_q = sin(\theta - \hat{\theta}) \tag{2.17}$$

which is obtained by the following terms:

- **Term 1:** we have

$$\cos\hat{\theta} V_a = \frac{2}{3}\cos\hat{\theta}\sin\theta \tag{2.18}$$

- **Term 2:** In this case, we have:

$$\frac{2}{3}\cos(\hat{\theta}-\frac{2\pi}{3})V_c = \frac{2}{3}\cos(\hat{\theta}-\frac{2\pi}{3})\sin(\theta-\frac{2\pi}{3})$$

$$= \frac{2}{3}\left[\cos\hat{\theta}\cos(\tfrac{2\pi}{3})+\sin\hat{\theta}\sin(\tfrac{2\pi}{3})\right]\left[\sin\theta\cos(\tfrac{2\pi}{3})-\cos\theta\sin(\tfrac{2\pi}{3})\right]$$

$$= \frac{2}{3}\left[-\tfrac{1}{2}\cos\hat{\theta}+\tfrac{\sqrt{3}}{2}\sin\hat{\theta}\right]\left[-\tfrac{1}{2}\sin\theta-\tfrac{\sqrt{3}}{2}\cos\theta\right]$$

which yields:

$$\frac{2}{3}\cos(\hat{\theta}-\frac{2\pi}{3})V_c = \frac{2}{3}\left[\tfrac{1}{4}\cos\hat{\theta}\sin\theta-\tfrac{3}{4}\sin\hat{\theta}\cos\theta+\tfrac{\sqrt{3}}{4}\cos\hat{\theta}\cos\theta-\tfrac{\sqrt{3}}{4}\sin\hat{\theta}\sin\theta\right] \tag{2.19}$$

- **Term 3:** We have:

$$\frac{2}{3}\cos(\hat{\theta}+\frac{2\pi}{3})V_b = \frac{2}{3}\cos(\hat{\theta}+\frac{2\pi}{3})\sin(\theta+\frac{2\pi}{3})$$

$$= \frac{2}{3}\left[\cos\hat{\theta}\cos(\tfrac{\pi}{3})-\sin\hat{\theta}\sin(\tfrac{\pi}{3})\right]\left[\sin\theta\cos(\tfrac{2\pi}{3})+\cos\theta\sin(\tfrac{2\pi}{3})\right]$$

$$= \frac{2}{3}\left[-\tfrac{1}{2}\cos\hat{\theta}-\tfrac{\sqrt{3}}{2}\sin\hat{\theta}\right]\left[-\tfrac{1}{2}\sin\theta+\tfrac{\sqrt{3}}{2}\cos\theta\right]$$

and we get the following:

$$= \frac{2}{3}\left[\tfrac{1}{4}\cos\hat{\theta}\sin\theta-\tfrac{3}{4}\sin\hat{\theta}\cos\theta-\tfrac{\sqrt{3}}{4}\cos\hat{\theta}\cos\theta+\tfrac{\sqrt{3}}{4}\sin\hat{\theta}\sin\theta\right]$$

Adding and simplifying the sum of these terms, we get the expression of V_q.

From above ((2.12), (2.16) and (2.17)), We conclude that conventional methods are equivalent where:

$$V_q = \frac{2}{3}p^{'} = \frac{1}{V_{max}}p^{''} \tag{2.20}$$

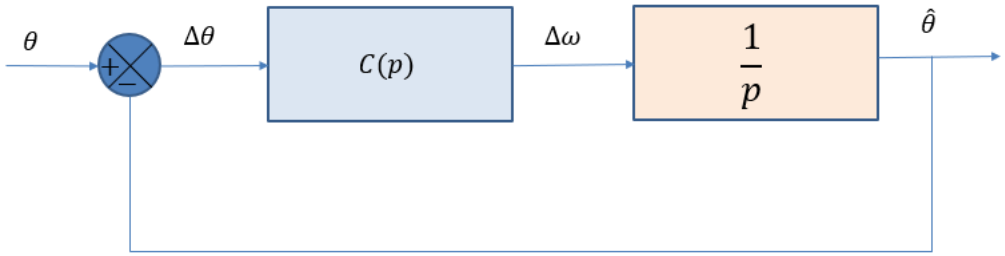


Figure 2.8: Block diagram of the closed loop system.

2.6 PI controller design

Assuming small variations $\sin \Delta\theta \approx \Delta\theta$, the closed loop system can be described by the following block diagram:
The system in open loop is described by the following transfer function:

$$F_{BO}(p) = C(p)\frac{1}{p} \tag{2.21}$$

where $C(p)$ is the PI transfer function which is given by:

$$C(p) = \frac{K_p p + K_i}{p} \tag{2.22}$$

where K_p and K_i are the controller parameters. From above, the closed loop system is described by the following transfer function:

$$F_{CL} = \frac{K_p p + K_i}{p^2 + K_p p + K_i} \tag{2.23}$$

The design of the PI parameters can be obtained by pole placement according to the control requirement (settling time, overshoot, etc)

2.7 Conclusion

In this chapter, we presented different conventional phase locked loop techniques for single phase systems as well as we studied different conventional methods for three phase systems. Moreover, we demonstrated that all PLL conventional methods are somehow equivalent.

Chapter 3

DDSRF PLL & Simulation results

3.1 Introduction

In this chapter we will see the Decoupled Double Synchronous Reference Frame PLL method (DDSRF-PLL) ,After we determined that all the conventional methods works authentically we will only choose one method wich is the dqPLL and compare it with the DDSRFPLL under different kinds of grid conditions to see witch PLL technique performs better than the other.

3.2 DDSRF-PLL for Power Converter Control

Decoupled double synchronous reference frame PLL (DDSRF-PLL) technique has the ability of fast and accurate detection of the positive-sequence component of an unbalanced voltage vector having both positive- and negative-sequence component, which later expresses on the double synchronous reference frame (DSRF) for detecting the positive-sequence component [13].

3.2.1 Double Synchronous Reference Frame

In Double synchronous reference frame PLL system, the U^s on Fig. 3.1 projected on two different rotating reference frames. The first one is dq^+ reference frame rotating with $\hat{\omega}$ frequency is synchronized with U^s_+ and second one is dq^- reference frame rotating with $-\hat{\omega}$ frequency is synchronized with U^s_- [14]. Fig. 3.1 shows the synchronous double

reference frame (SDRF) and the representation of voltage vectors with the reference axes. The expression U^s on these reference frames is:

$$U^+ = \begin{bmatrix} U_d^+ \\ U_q^+ \end{bmatrix} = T_{dq}^+ U^s \tag{3.1}$$

$$U^- = \begin{bmatrix} U_d^- \\ U_q^- \end{bmatrix} = T_{dq}^- U^s \tag{3.2}$$

where the superscript '+' represent the vectors rotating with a positive angular frequency ω and '-' represent the vectors rotating with a negative angular frequency $-\omega$, respectively.

The synchronous transformation matrices T_dq^+ and T_dq^- are,

$$T_{dq}^+ = \begin{bmatrix} \cos\hat{\theta} & \sin\hat{\theta} \\ -\sin\hat{\theta} & \cos\hat{\theta} \end{bmatrix} \tag{3.3}$$

$$T_{dq}^- = \begin{bmatrix} \cos\hat{\theta} & -\sin\hat{\theta} \\ \sin\hat{\theta} & \cos\hat{\theta} \end{bmatrix} \tag{3.4}$$

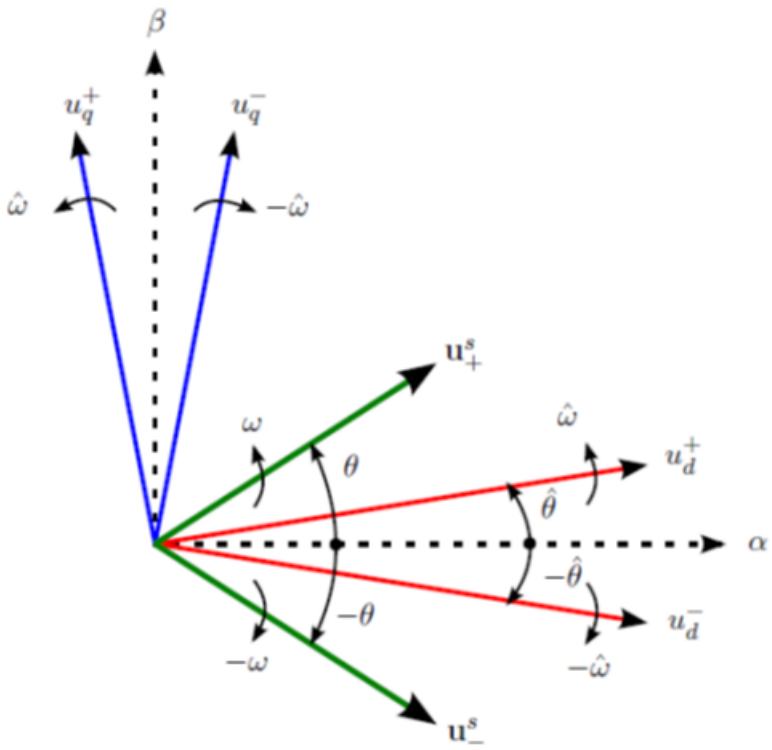


Figure 3.1: SDRF. Representation of voltage vectors with the reference axes

where: $\hat{\theta} = \int \hat{\omega}\, dt$ holds during transients.

Now from (3.1), (3.2), (3.3) and (3.4) we get,

$$U_d^+ = U_+ \cos(\omega t - \hat{\theta}) + U_- \cos(-\omega t + \Phi^{-1} - \hat{\theta}) \tag{3.5}$$

$$U_d^- = U_+ \cos(\omega t + \hat{\theta}) + U_- \cos(-\omega t + \Phi^{-1} + \hat{\theta}) \tag{3.6}$$

$$U_q^+ = U_+ \sin(\omega t - \hat{\theta}) + U_- \sin(-\omega t + \Phi^{-1} - \hat{\theta}) \tag{3.7}$$

$$U_q^- = U_+ \sin(\omega t + \hat{\theta}) + U_- \sin(-\omega t + \Phi^{-1} + \hat{\theta}) \tag{3.8}$$

we can express (3.5) to (3.8) in matrices as:

$$U^+ = \begin{bmatrix} U_d^+ \\ U_q^+ \end{bmatrix} = U_+ \begin{bmatrix} \cos(\omega t - \hat{\theta}) \\ \sin(\omega t - \hat{\theta}) \end{bmatrix} + U_- \begin{bmatrix} \cos(-\omega t + \Phi^{-1} - \hat{\theta}) \\ \sin(-\omega t + \Phi^{-1} - \hat{\theta}) \end{bmatrix} \tag{3.9}$$

$$U^- = \begin{bmatrix} U_d^- \\ U_q^- \end{bmatrix} = U_+ \begin{bmatrix} \cos(\omega t + \hat{\theta}) \\ \sin(\omega t + \hat{\theta}) \end{bmatrix} + U_- \begin{bmatrix} \cos(-\omega t + \Phi^{-1} + \hat{\theta}) \\ \sin(-\omega t + \Phi^{-1} + \hat{\theta}) \end{bmatrix} \tag{3.10}$$

By the correct tuning of the control loop, the estimated angle $\hat{\theta}$ of the positive sequence voltage vector should be equal to the real angle of this vector, θ. So, $\hat{\theta} = \int \hat{\omega}\, dt \approx \theta = \int \omega\, dt$ will result the following voltages from (3.5) and (3.6):

$$U_d^+ = U_+ + U_- \cos(-2\omega t + \Phi^{-1}) \tag{3.11}$$

$$U_d^- = U_+ \cos(2\omega t) + U_- \cos(\Phi^{-1}) \tag{3.12}$$

where $(-\omega t + \Phi^{-1} - \hat{\theta}) \approx (-2\omega t + \Phi^{-1})$ and $\cos(\omega t - \hat{\theta}) \approx 0$ approximations has been made. Now, from (3.7) and (3.8):

$$U_q^+ = U_- \sin(-2\omega t + \Phi^{-1}) \tag{3.13}$$

$$U_q^- = U_+ \sin(2\omega t + \Phi^{-1}) + U_- \sin(\Phi^{-1}) \tag{3.14}$$

where $(-\omega t + \Phi^{-1} - \hat{\theta}) \approx (-2\omega t + \Phi^{-1})$ and $\sin(\omega t - \hat{\theta}) \approx 0$ approximations has been made. Now, from (3.9) and (3.10) will be respectively:

$$u^+ = \begin{bmatrix} U_d^+ \\ U_q^+ \end{bmatrix} = U_+ \begin{bmatrix} 1 \\ 0 \end{bmatrix} + U_- \begin{bmatrix} \cos(-2\omega t + \Phi^{-1}) \\ \sin(-2\omega t + \Phi^{-1}) \end{bmatrix} \tag{3.15}$$

$$u^- = \begin{bmatrix} U_d^- \\ U_q^- \end{bmatrix} = U_+ \begin{bmatrix} \cos(2\omega t) \\ \sin(2\omega t) \end{bmatrix} + U_- \begin{bmatrix} \cos(\Phi^{-1}) \\ \sin(\Phi^{-1}) \end{bmatrix} \tag{3.16}$$

In (3.15) and (3.16), the dc values on the u^+ and the u^- axes depends on the amplitude of U_+ and U_-, respectively. The term 2ω represents the oscillation as a result of coupling between two axes; because the vectors are rotating in opposite direction.

This oscillation is acting as a perturbation for the detection of U_+ and U_-. These oscillations can be attenuated by using traditional filtering techniques. But the grid condition requires high accuracy and excellent dynamic response like dynamic voltage restorers (DVR) under unbalance, conventional SRF-PLL technique is not an appropriate solution for the control of power converters.

3.2.2 The Decoupling Network

A voltage vector U^s having two generic components rotating with $n\omega$ and $m\omega$ frequencies respectively, where n and m can be either positive or negative and ω is the fundamental frequency can be expressed as,

$$u^s = u_n^s + u_m^s = U_n \begin{bmatrix} \cos(n\omega t + \Phi^n) \\ \sin(n\omega t + \Phi^n) \end{bmatrix} + U_m \begin{bmatrix} \cos(m\omega t + \Phi^m) \\ \sin(m\omega t + \Phi^m) \end{bmatrix} \tag{3.17}$$

Two rotating reference frames, dq^n reference frame with angular position $n\hat{\theta}$ will be synchronized with u_n^s and second one is dq^m reference frame with angular position $m\hat{\theta}$ will be synchronized with u_m^s. By the feasible tuning of the control loop, a perfect synchronization of the PLL is possible and the reference frames can be written as:

$$u^n = \begin{bmatrix} u_d^n \\ u_q^n \end{bmatrix} = \begin{bmatrix} \overline{u_d^n} \\ \overline{u_q^n} \end{bmatrix} + \begin{bmatrix} \widetilde{u_d^n} \\ \widetilde{u_q^n} \end{bmatrix} \tag{3.18}$$
$$= U_n \begin{bmatrix} \cos\Phi^n \\ \sin\Phi^n \end{bmatrix} + U_m \cos\Phi^m \begin{bmatrix} \cos((n-m)\omega t) \\ -\sin((n-m)\omega t) \end{bmatrix} + U_m \sin\Phi^m \begin{bmatrix} \sin((n-m)\omega t) \\ \cos((n-m)\omega t) \end{bmatrix}$$

$$u^m = \begin{bmatrix} u_d^m \\ u_q^m \end{bmatrix} = \begin{bmatrix} \overline{u_d^m} \\ \overline{u_q^m} \end{bmatrix} + \begin{bmatrix} \widetilde{u_d^m} \\ \widetilde{u_q^m} \end{bmatrix} \tag{3.19}$$
$$= U_m \begin{bmatrix} \cos\Phi^m \\ \sin\Phi^m \end{bmatrix} + U_n \cos\Phi^n \begin{bmatrix} \cos((n-m)\omega t) \\ \sin((n-m)\omega t) \end{bmatrix} + U_n \sin\Phi^n \begin{bmatrix} -\sin((n-m)\omega t) \\ \cos((n-m)\omega t) \end{bmatrix}$$

From (3.18) and (3.19) it is clearly seen that the amplitude of ac terms in dq^n depends on the dc terms of the signal on the dq^m axes and vice versa. For cancelling out the oscillating term in the dq^n axes, the decoupling cell in Fig. 3.2 can be used [55]. Also, For cancelling out the oscillating term in the dq^m axes, decoupling cell in Fig. 3.3 can be used, which is similar to the Fig. 3.2 but only the position of m and n needs to be interchanged. Now, for estimating the dc values of the positive and negative reference frames, a cross-feedback decoupling network can be used as shown in Fig. 3.4. The LPF block is a low pass filter can be represented as [55],

$$LPF = \frac{\omega_f}{p + \omega_f} \tag{3.20}$$

where ω_f is the cutoff frequency of the LPF.

The equations for both decoupling cells can be written as,

$$\overline{u_d^n} = \frac{\omega_f}{p + \omega_f} \left(u_d^n - \overline{u_d^m} \cos((n-m)\hat{\theta}) - \overline{u_q^m} \sin((n-m)\hat{\theta}) \right) \tag{3.21}$$

$$\overline{u_q^n} = \frac{\omega_f}{p + \omega_f} \left(u_q^n - \overline{u_d^m} \sin((n-m)\hat{\theta}) - \overline{u_q^m} \cos((n-m)\hat{\theta}) \right) \tag{3.22}$$

$$\overline{u_d^m} = \frac{\omega_f}{p + \omega_f} \left(u_d^m - \overline{u_d^n} \cos((n-m)\hat{\theta}) - \overline{u_q^n} \sin((n-m)\hat{\theta}) \right) \tag{3.23}$$

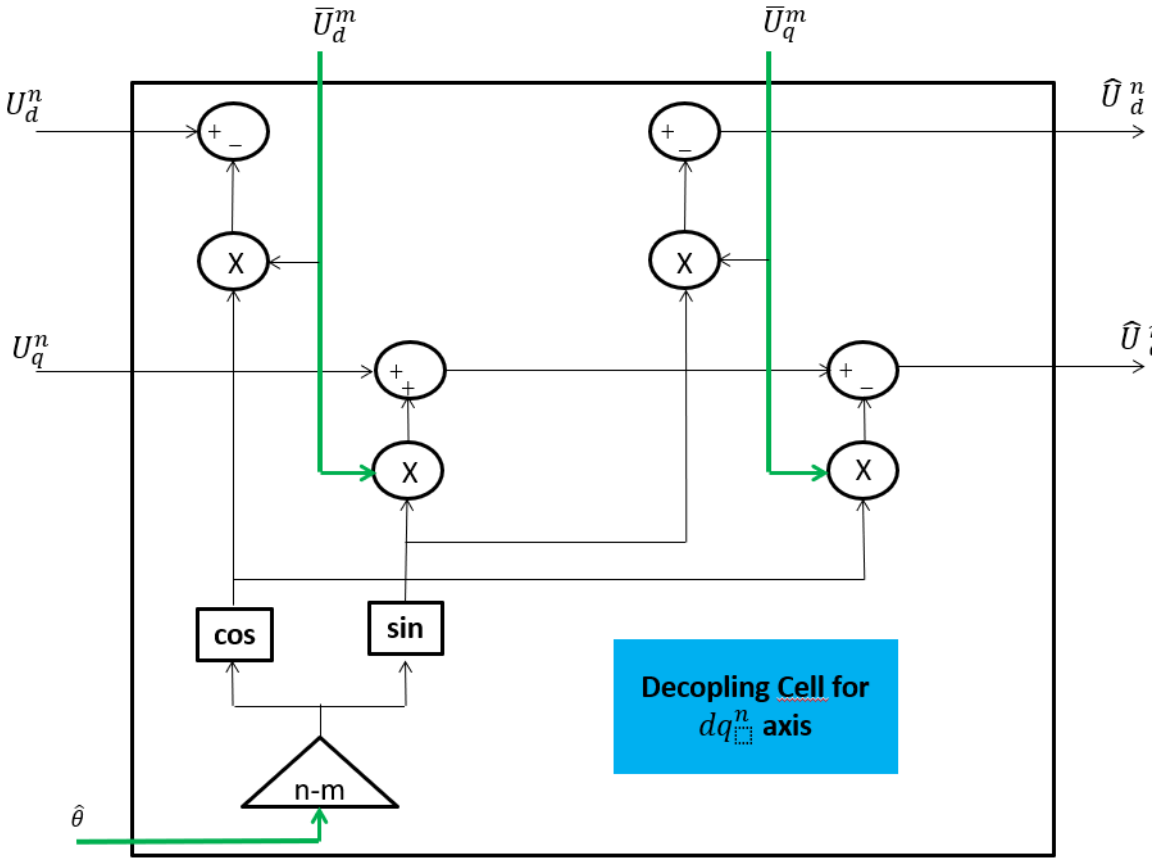


Figure 3.2: Decoupling cell for cancelling the oscillation on dq^n axes

$$\overline{u_q^m} = \frac{\omega_f}{p+\omega_f}\left(u_q^m - \overline{u_d^n}\sin((n-m)\hat{\theta}) - \overline{u_q^n}\cos((n-m)\hat{\theta})\right) \tag{3.24}$$

Now considering an unbalance voltage during a grid fault, consisting of positive and negative sequence components at fundamental frequency, where $n = 1$ and $m = -1$, (3.17) can be represented as:

$$u^s = u^s_{+1} + u^s_{-1} = U_{+1}\begin{bmatrix}\cos(+\omega t + \Phi^{+1})\\ \sin(+\omega t + \Phi^{+1})\end{bmatrix} + U_{-1}\begin{bmatrix}\cos(-\omega t + \Phi^{-1})\\ \sin(-\omega t + \Phi^{-1})\end{bmatrix} \tag{3.25}$$

Then (3.18) will be:

$$u^{+1} = U_{+1}\begin{bmatrix}\cos\Phi^{+1}\\ \sin\Phi^{+1}\end{bmatrix} + U_{-1}\cos\Phi^{-1}\begin{bmatrix}\cos(2\omega t)\\ -\sin(2\omega t)\end{bmatrix} + U_{-1}\sin\Phi^{-1}\begin{bmatrix}\sin(2\omega t)\\ \cos(2\omega t)\end{bmatrix} \tag{3.26}$$

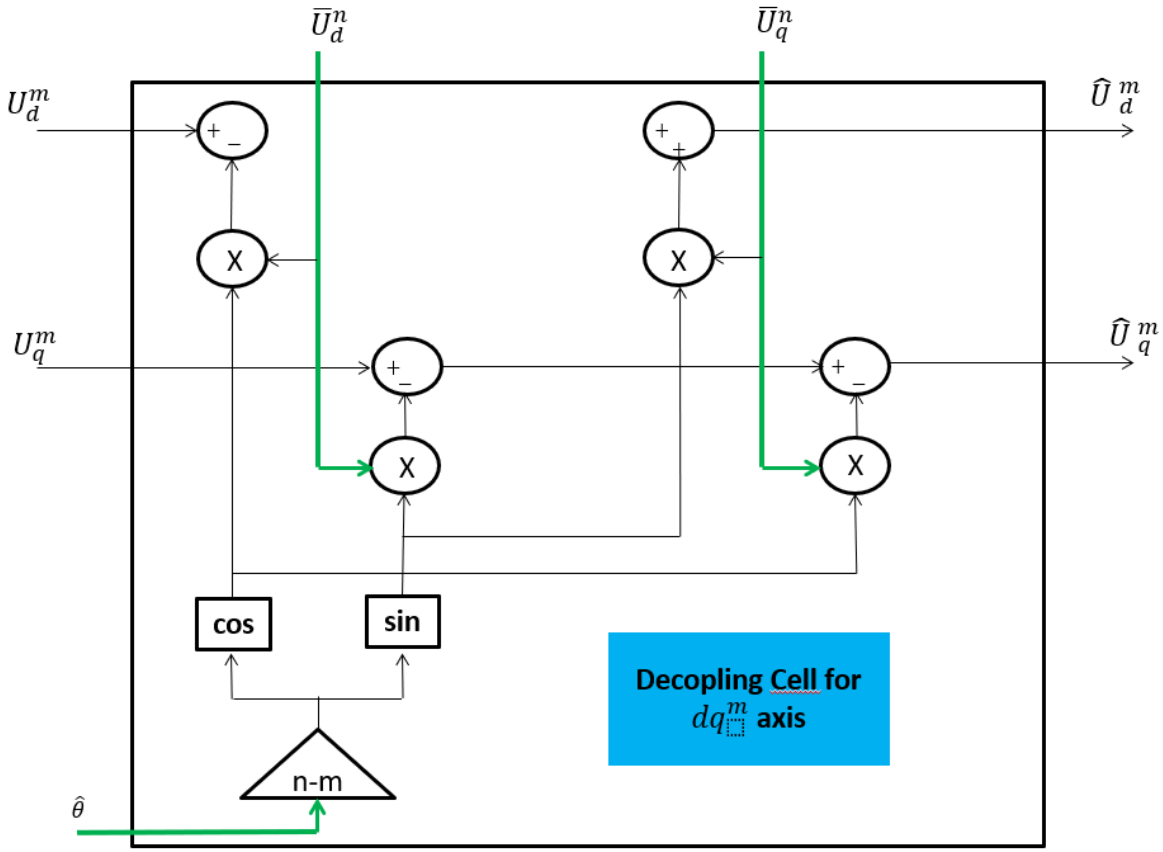


Figure 3.3: Decoupling cell for cancelling the oscillation on dq^m axes.

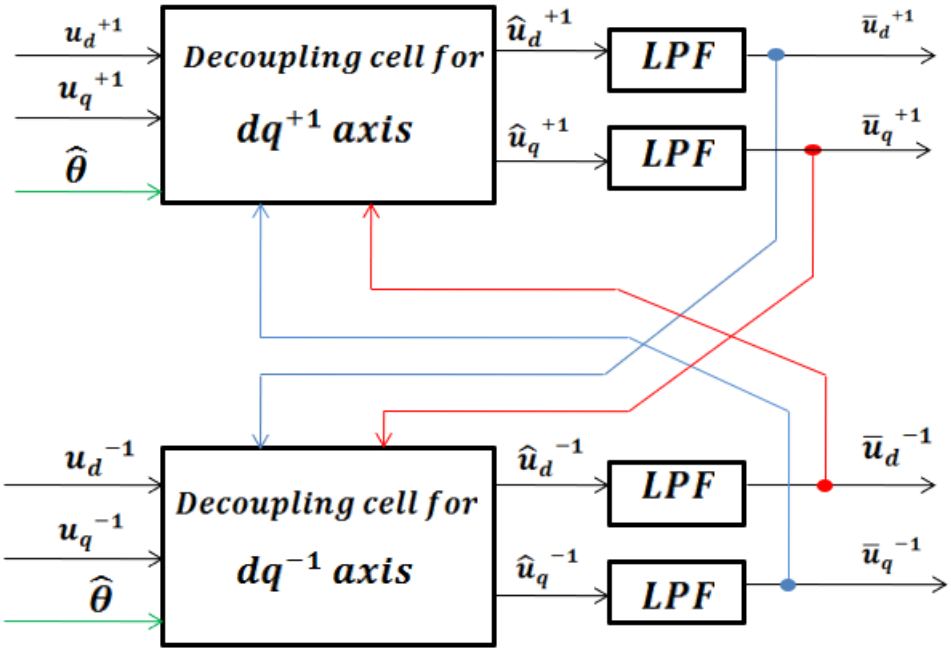


Figure 3.4: Decoupling network of dq^n and dq^m reference frame.

And (3.19) will be:

$$u^m = \begin{bmatrix} u_d^m \\ u_q^m \end{bmatrix} = \begin{bmatrix} \overline{u_d^m} \\ \overline{u_q^m} \end{bmatrix} + \begin{bmatrix} \widetilde{u_d^m} \\ \widetilde{u_q^m} \end{bmatrix} \tag{3.27}$$
$$= U_m \begin{bmatrix} \cos\Phi^m \\ \sin\Phi^m \end{bmatrix} + U_n \cos\Phi^n \begin{bmatrix} \cos((n-m)\omega t) \\ \sin((n-m)\omega t) \end{bmatrix} + U_n \sin\Phi^n \begin{bmatrix} -\sin((n-m)\omega t) \\ \cos((n-m)\omega t) \end{bmatrix}$$

Equations (3.21)-(3.24) can be written as respectively

$$\overline{u_d^{+1}} = \frac{\omega_f}{p+\omega_f}\left(u_d^{+1} - \overline{u_d^{-1}}\cos(2\hat{\theta}) - \overline{u_q^{-1}}\sin(2\hat{\theta})\right) \tag{3.28}$$

$$\overline{u_q^{+1}} = \frac{\omega_f}{p+\omega_f}\left(u_q^{+1} - \overline{u_d^{-1}}\sin(2\hat{\theta}) - \overline{u_q^{-1}}\cos(2\hat{\theta})\right) \tag{3.29}$$

$$\overline{u_d^{-1}} = \frac{\omega_f}{p+\omega_f}\left(u_d^{-1} - \overline{u_d^{+1}}\cos(2\hat{\theta}) - \overline{u_q^{+1}}\sin(2\hat{\theta})\right) \tag{3.30}$$

$$\overline{u_q^{-1}} = \frac{\omega_f}{p+\omega_f}\left(u_q^{-1} - \overline{u_d^{+1}}\sin(2\hat{\theta}) - \overline{u_q^{+1}}\cos(2\hat{\theta})\right) \tag{3.31}$$

The decoupling network in Fig. 3.5 completely cancels out the double frequency oscillations at 2ω on the dq^{+1} and dq^{-1} reference frame signals; the control loop bandwidth is no need to be reduced and the real amplitude of the unbalanced input voltage sequence components can be exactly detected [5]. With these decoupling networks, the signal with frequency 2ω does not arrive in the PI controller input, and hence the system bandwidth can be increased for achieving a better dynamic behavior.

3.3 Simulation results and discussions

In our simulation, initially, we will choose balanced grid voltages with 220V RMS and a 50Hz fundamental frequency. We will study the difference between conventional methods then we check the performance of each PLL under three cases of grid conditions:

- **Case 1**: balanced and unbalanced grid condition (frequency variation).
- **Case 2**: unbalanced grid condition: amplitude variation.

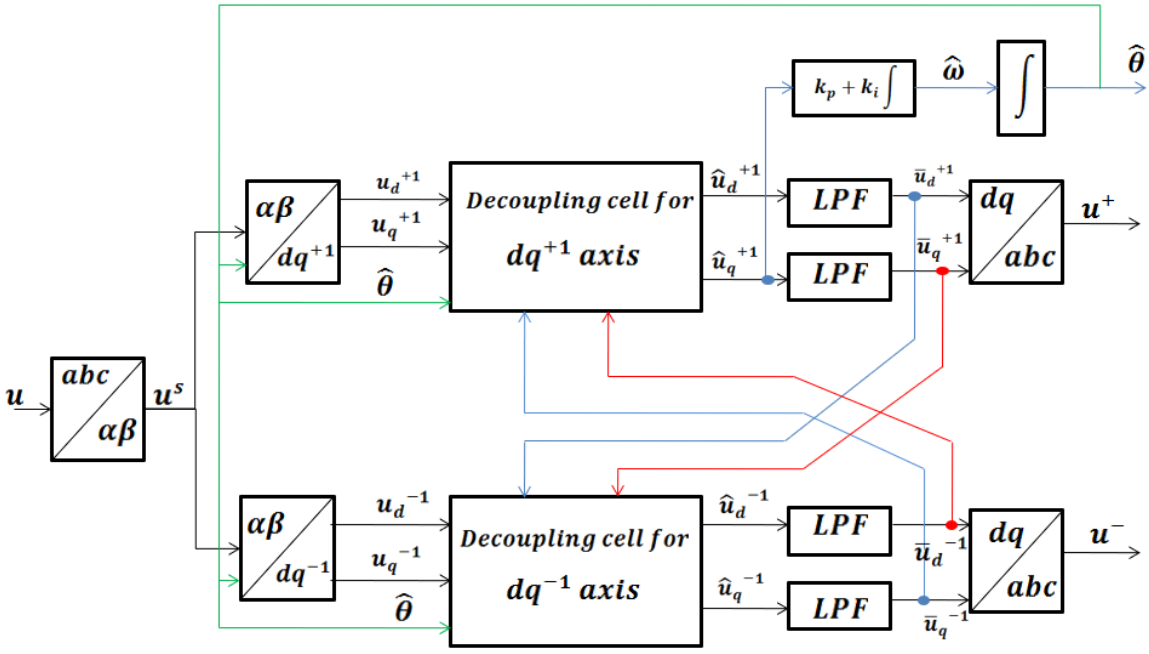


Figure 3.5: Block diagram of the decoupled double synchronous reference frame PLL (DSRF-PLL).

- **Case 3**: unbalanced grid condition: phase angle variation.

3.3.1 Equivalence between conventional methods

In this part, we will show that choosing controller parameters for each PLL method with respect to the equivalence formulae given by (2.20), we can get the same simulations results.

Figures 3.6, 3.7 and 3.8 illustrate phase a voltage, frequency and phase angle of PLL and grid signals, respectively. We remark that all PLLs guarantee the estimation of the phase angle (hence frequency) of the grid voltages. Moreover, all methods provide the same result which confirm mathematical proofs in the previous chapter.

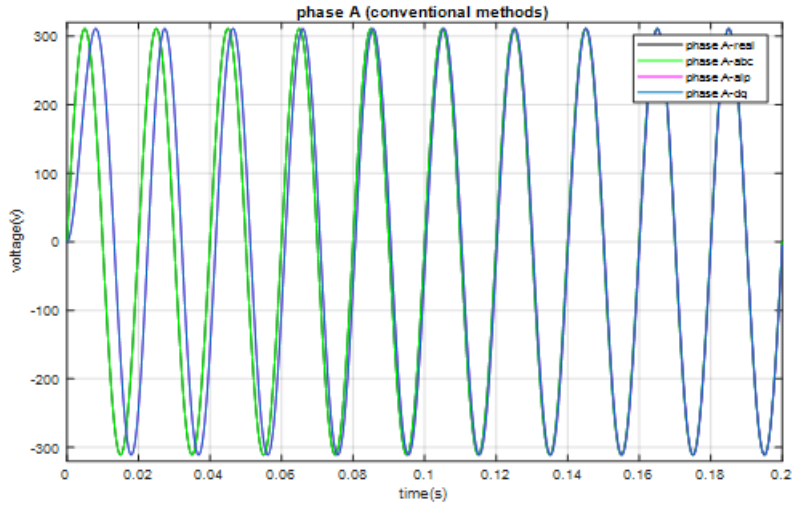


Figure 3.6: phase A of the conventional PLL methods and three phase system

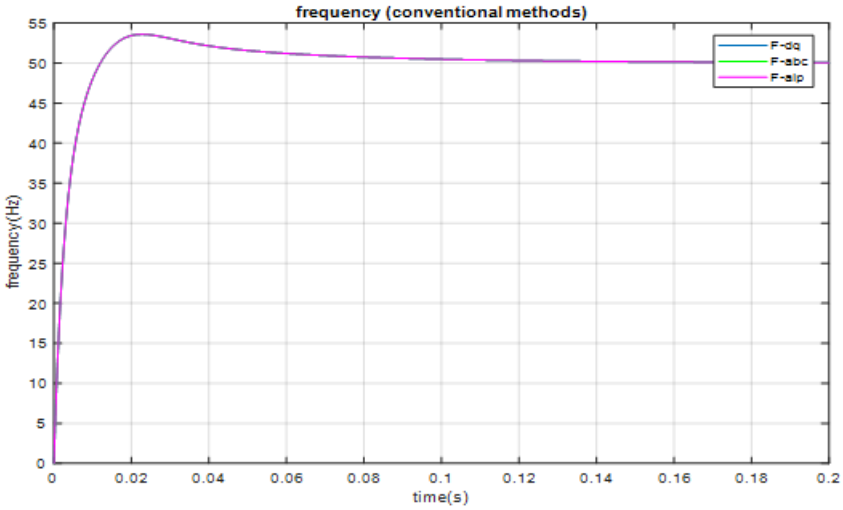


Figure 3.7: frequency of the conventional PLL methods.

3.3.2 Robustness under frequency variation

In this scenario, we are going to consider the following three phase system:

$$V_a = V_{max}\sin(\omega t) \tag{3.32}$$

$$V_b = V_{max}\sin(\omega t - \frac{2\pi}{3}) \tag{3.33}$$

$$V_c = V_{max}\sin(\omega t + \frac{2\pi}{3}) \tag{3.34}$$

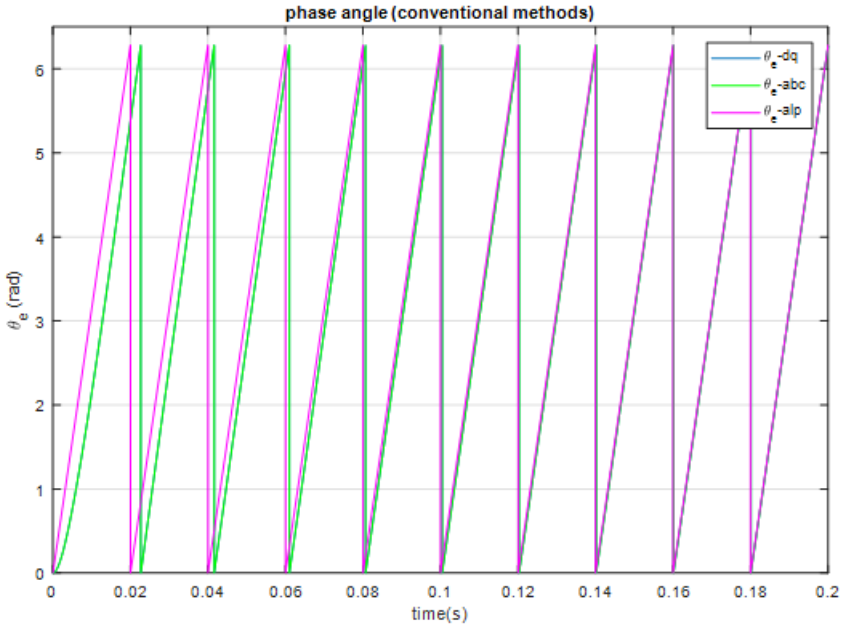


Figure 3.8: Phase angle of the conventional PLL methods.

where $V_{max} = 220\sqrt{2}V$ and

$$f = \begin{cases} 50Hz & 0 \leq t < 0.8s \\ 55Hz & 0.8 \leq t < 1.6s \\ 45Hz & 1.6 \leq t < 2.4s \end{cases} \tag{3.35}$$

The controller parameters for both methods (dq-PLL and DDSRF-PLL) are chosen the same: $K_p = 1$ and $K_i = 20$.

Figure 3.9 represents the estimated frequency of DDSRF-PLL and dq-PLL methods under frequency variation. From Figure 3.10, we can observe that the settling time is the same for both methods. However, we can remark that DDSRF-PLL method has oscillations that disappear after 0.1s but this does not affect the phase estimation.

Figure 3.11 and Figure 3.12 represent the estimated phase angle of DDSRF-PLL and dq-PLL methods under frequency variation. We note that the response time is the same both methods guarantee a good of estimation of the phase angle of grid voltages.

From above, we conclude that **dq-PLL and DDSRF-PLL methods are efficient with respect to frequency variation**.

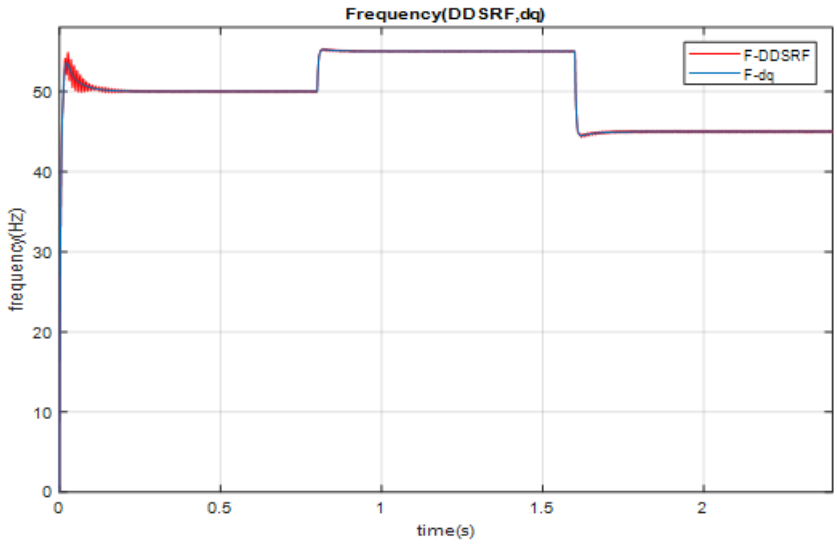


Figure 3.9: Performance of different PLLs under frequency variation.

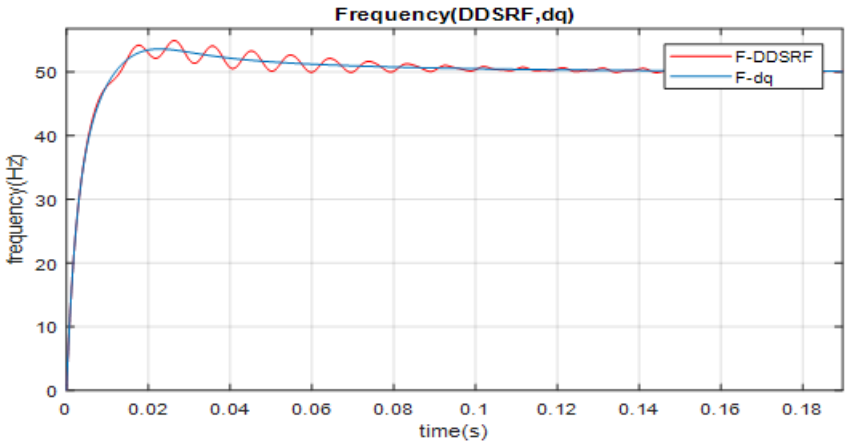


Figure 3.10: Zoom version of performance of different PLLs under frequency variation.

3.3.3 Robustness under amplitude variation

In this case, we are going to consider the following three phase system:

$$V_a = V_{max}\sin(\omega t) \tag{3.36}$$

$$V_b = V_{max}\sin(\omega t - \frac{2\pi}{3}) \tag{3.37}$$

$$V_c = V_{max}\sin(\omega t + \frac{2\pi}{3}) \tag{3.38}$$

where $f = 50\text{Hz}$ and

$$V_{max} = \begin{cases} 245\sqrt{2} & 0 \leq t < 0.8s \\ 200\sqrt{2} & 0.8 \leq t < 1.6s \end{cases} \tag{3.39}$$

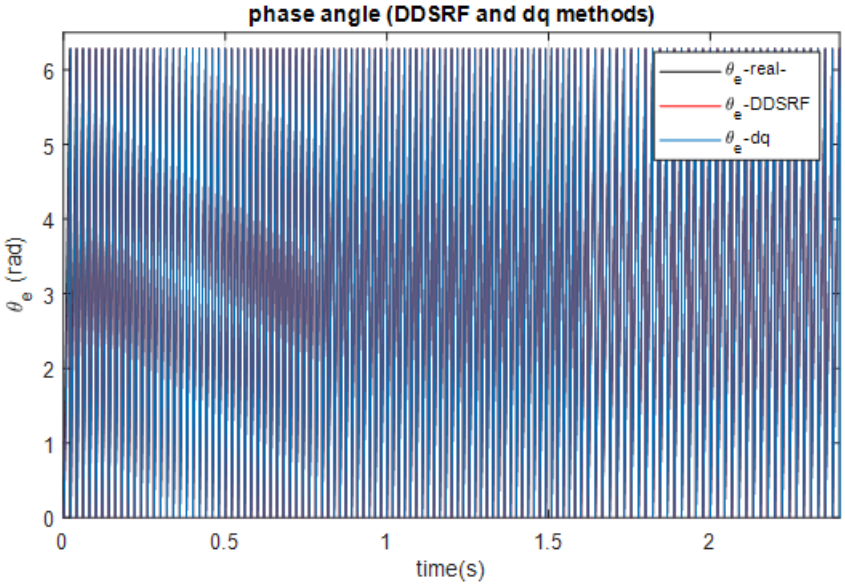


Figure 3.11: Phase angle θ and θ_e of different PLLs under frequency variation

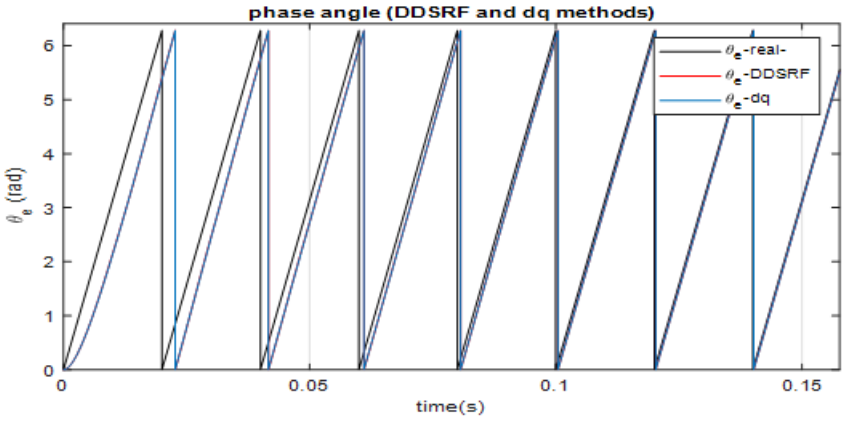


Figure 3.12: Zoom version of phase angle θ and θ_e of different PLLs under frequency variation

Figure 3.13 represents the estimated frequency of DDSRF-PLL and dq-PLL methods under frequency variation. The two methods are not affected by amplitude variations of grid voltages. This is confirmed by convergence of the PLL phase angle to the grid angle as shown in Figure 3.14 and the zoom version in Figure 3.15.

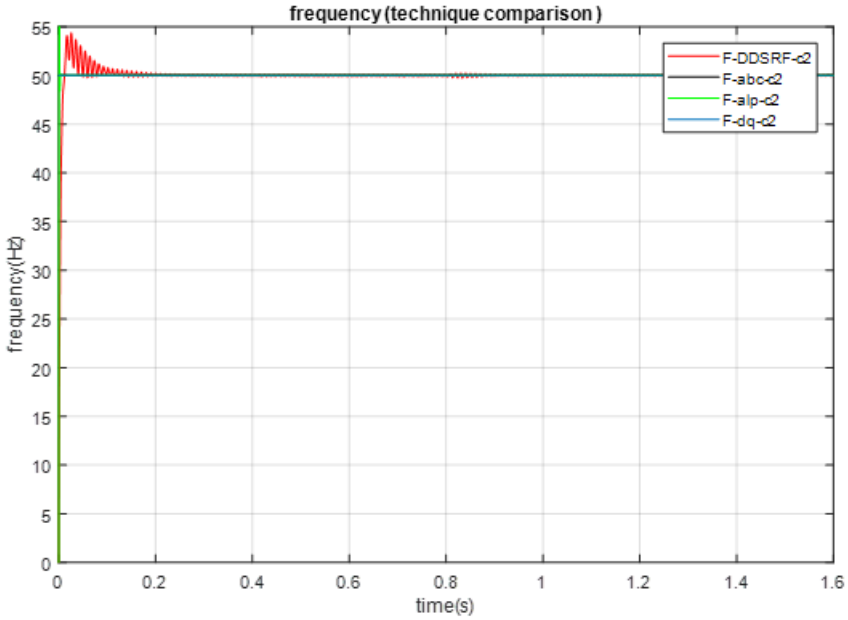


Figure 3.13: Performance of different PLLs under amplitude variation.

3.3.4 Robustness under phase shift variation

In this case, we are going to consider the following three phase system:

$$V_a = V_{max}\sin(\omega t) \tag{3.40}$$

$$V_b = V_{max}\sin(\omega t - \frac{2\pi}{3}) \tag{3.41}$$

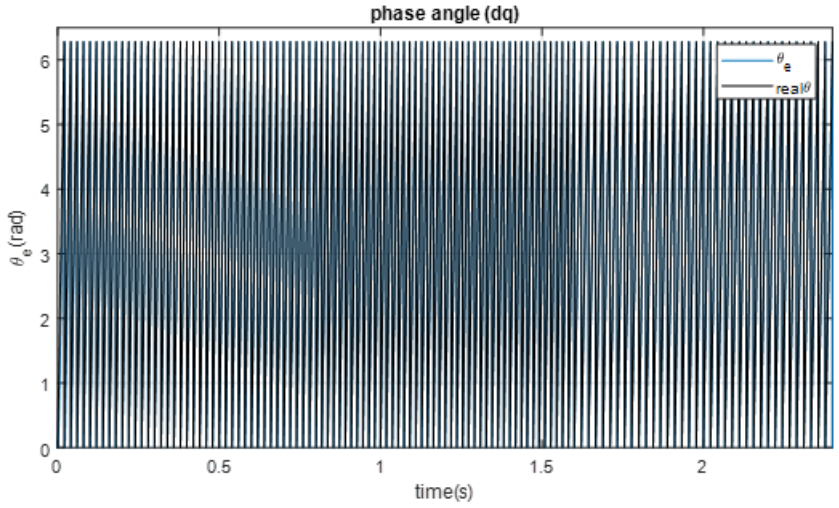
$$V_c = V_{max}\sin(\omega t + \frac{2\pi}{3}) \tag{3.42}$$

where $f = 50\text{Hz}$, $V_{max} = 220\sqrt{2}$ and

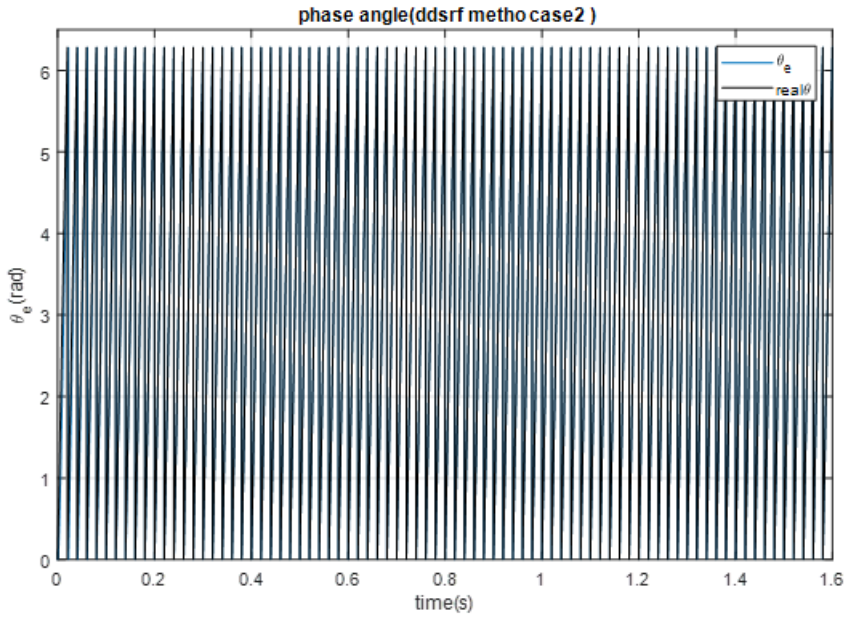
$$phase - shift = \begin{cases} 1.1 & 0 \leq t < 0.8s \\ 0.9 & 0.8 \leq t < 1.6s \end{cases} \tag{3.43}$$

Simulation results are shown in Figure 3.16 for frequency evolution and Figure 3.17 for phase angle estimation. From these results, we remark that *dq*-PLL method is affected by phase shift variation with the remarkable oscillations in the estimated frequency compared to DDSRF-PLL. This also confirmed by an error in phase angle estimation which is shown in the Zoom version.

Last but not least, the simulation results proved that the two methods give authentically results under balanced grid condition but in unbalanced grid condition we



(a) Phase angle θ and θ_e of dq-PLL



(b) Phase angle θ and θ_e of DDSRF-PLL

Figure 3.14: Performance of different PLLs under amplitude variation.

saw that the DDSRP-PLL performed better compared to conventional PLLs. This may allow us to consider the DDSRF-PLL as suitable solution for grid synchronization grid. However, we should note that DDSRF-PLL has a complex structure compared to conventional PLLs.

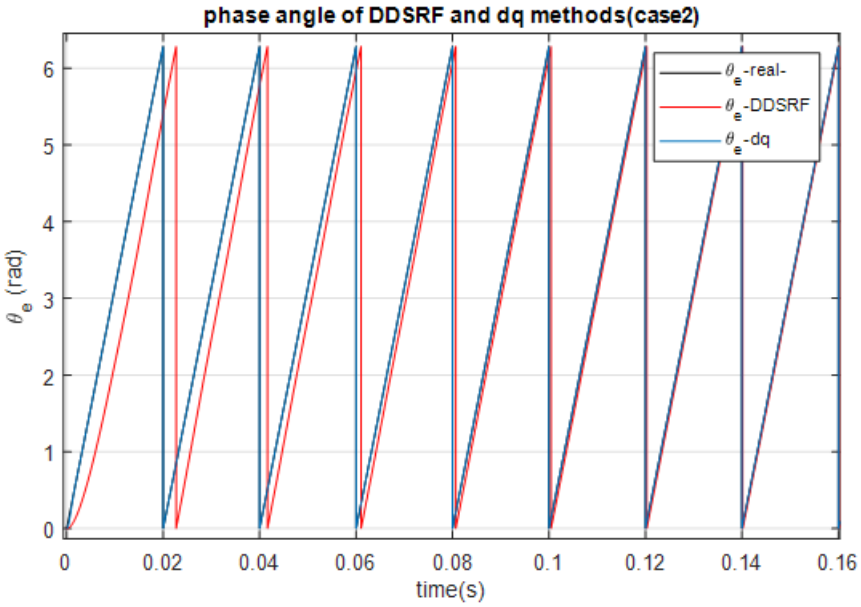


Figure 3.15: Zoom version of phase angle of different PLLs under amplitude variation.

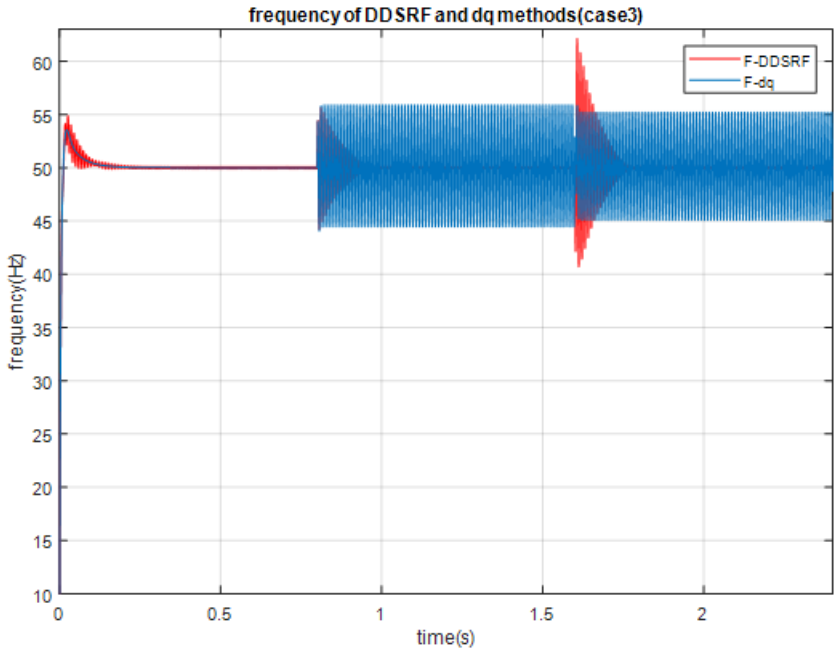


Figure 3.16: Performance of different PLLs under phase shift variation.

3.4 Conclusion

In this chapter, we have presented the double decoupled synchronous frame PLL, denoted DDSRF-PLL. We also implemented different PLL methods in Simulink/Matlab

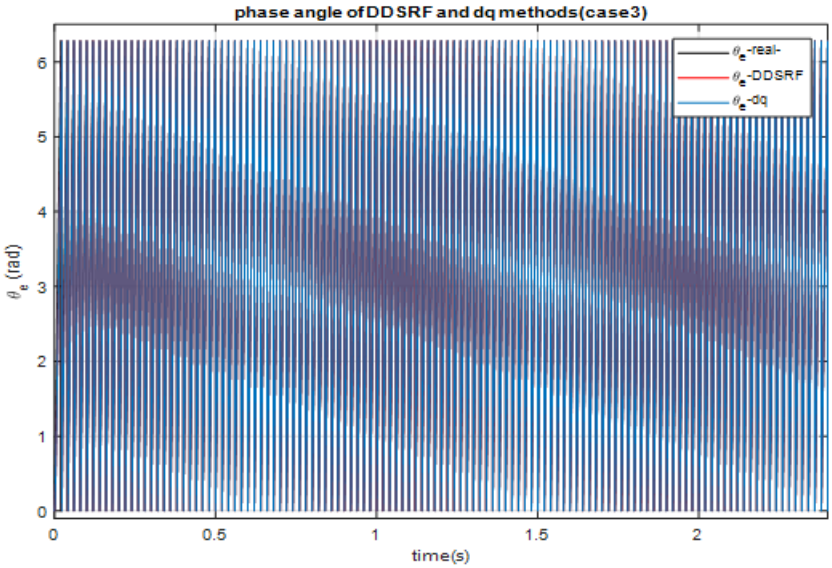


Figure 3.17: Phase angle θ and θ_e of DDSRF-PLL under phase shift variation.

and tested their performance under balanced and unbalanced grid conditions. Despite the complexity of the DDSRF-PLL, it is quiet insensitive to phase shift variations compared to conventional methods.

General Conclusion

In this master project, we dealt with phase locked loop techniques dedicated to power converters for grid synchronization. In the first chapter, we presented generalities about phase locked loop where we highlight the basic structure, applications and some technical terms.

The second chapter is the one that introduce us to the PLL structure for grid-connected converters. We started with single phase system where we presented two methods: 1) PLL based on T/4 delay, 2) PLL based on Inverse Park's Transform. Then, we moved to the three phase system where we highlighted different conventional PLL structures. This depends on which frame we use. We have abc-frame PLL, $\alpha\beta$-frame PLL and dq-PLL frame. We proved mathematically that these methods are equivalent and we ended the chapter by PI-controller design based on closed loop transfer function.

In the third chapter, we introduced a more complex and efficient PLL method, known as decoupled double synchronous frame PLL. Then, we moved to the simulation and discussions part. We started by proving that the conventional methods are equivalent under balanced grid conditions and we considered the dq-PLL method for the comparative study. The latter is done under balanced and unbalanced grid conditions for both dq-PLL and DDSRF-PLL methods.

Simulation results shows the efficiency of PLL methods under different grid conditions. However, DDSRF-PLL is insensitive to phase shift variations which is observed by the damped response of the estimated frequency.

This master project is an introduction to the design of more advanced control strategies that will treat this problem in rigorous manner. It is true that we highlighted existing methods and we investigated the difference between them. But, we can do

better using methods like *slidingmodecontrol* or even design efficient observers for measured data (voltages in our case).

Appendix A

Clarke & Park transformations

A.1 The Clarke Transformation

The $\alpha\beta$ transformation or the Clarke transformation maps the three-phase instantaneous voltages in the abc phases, V_a, V_b, and V_c, into the instantaneous voltages on the $\alpha\beta$ axes. The Clarke Transformation and its inverse transformation of three-phase voltages are given by:

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \sqrt{\frac{1}{2}} & \sqrt{\frac{1}{2}} & \sqrt{\frac{1}{2}} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{A.1}$$

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 & -\frac{1}{\sqrt{2}} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \\ V_0 \end{bmatrix} \tag{A.2}$$

A.2 The Park Transformation

The three-phase quantities are translated from the three-phase reference frame to the two-axis orthogonal stationary reference frame as follows:

$$\begin{bmatrix} V_d \\ V_q \\ V_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \sin\hat{\theta} & \sin(\hat{\theta} - \frac{2\pi}{3}) & \sin(\hat{\theta} + \frac{2\pi}{3}) \\ \cos\hat{\theta} & \cos(\hat{\theta} - \frac{2\pi}{3}) & \cos(\hat{\theta} + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{A.3}$$

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