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Theme

Design and Implementation of Active Disturbance Rejection Control (ADRC) for DC/DC Converter

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يتناول هذا العمل التحكم في محولات التيار المستمر (DC/DC) باستخدام تقنية التحكم الفعال في رفض الاضطرابات (ADRC). تم دراسة كل من محول Buck ومحول Boost وفقًا لاستراتيجيتين: التحكم المتتالي (Cascade ADRC) والتحكم المعتمد على الخطأ (Error-based ADRC). أظهرت نتائج المحاكاة باستخدام MATLAB/Simulink قدرة المتحكم على رفض الاضطرابات، وتتبع الإشارة المرجعية، والحفاظ على الاستقرار تحت تأثير تغيرات جهد الدخل والحمل.

أظهر التحكم المتتالي استجابة سريعة ومتانة قوية، بينما تميز التحكم المعتمد على الخطأ ببنية أبسط وإشارات تحكم سلسة. وقد تم أيضًا اختبار محول Buck تجريبيًا باستخدام منصة dSPACE 1104. وأكدت النتائج في الزمن الحقيقي فعالية تقنية ADRC في التطبيقات العملية، مما يدل على ملاءمتها لأنظمة إلكترونيات الطاقة.

الكلمات المفتاحية: محول تيار مستمر/تيار مستمر ؛(DC/DC) محول ؛"Buck" محول ؛"Boost" التحكم الفعّال في رفض الاضطرابات ؛(ADRC) المراقب الموسع للحالة ؛(ESO) التحكم المتتالي؛ التحكم المعتمد على الخطأ بـ ؛ADRC متحكم .PI

Abstract

This work investigates the control of DC/DC converters using Active Disturbance Rejection Control (ADRC). Both Buck and Boost converters are studied under two strategies: cascade ADRC and error-based ADRC. Simulation results in MATLAB/Simulink demonstrate the controllers' ability to reject disturbances, track references, and maintain stability under input voltage and load variations.

Cascade ADRC showed strong robustness and fast response, while error-based ADRC offered simpler structure and smooth control signals. The Buck converter was further tested experimentally using a dSPACE 1104 platform. Real-time results confirmed the effectiveness of ADRC in practical scenarios, highlighting its suitability for power electronics applications.

Keywords: DC/DC converter; Buck-converter; Boost-converter; ADRC;ESO; Cascade control; Error-based ADRC; PI.

Resumé

Ce travail étudie le contrôle des convertisseurs DC/DC à l'aide du contrôle actif de rejet de perturbation (ADRC). Les convertisseurs Buck et Boost sont étudiés selon deux stratégies: l'ADRC en cascade et l'ADRC basé sur les erreurs. Les résultats de la simulation dans MATLAB/Simulink démontrent la capacité des contrôleurs à rejeter les perturbations, à suivre les références et à maintenir la stabilité sous les variations de tension d'entrée et de charge.

Cascade ADRC a montré une forte robustesse et une réponse rapide, tandis que l'ADRC basé sur les erreurs offrait une structure plus simple et des signaux de contrôle lisses. Le convertisseur Buck a été testé expérimentalement à l'aide d'une plateforme dSPACE

1104. Les résultats en temps réel ont confirmé l'efficacité de l'ADRC dans des scénarios pratiques, soulignant son adéquation pour les applications de l'électronique de puissance.
Mots-clés: Convertisseur DC/DC ; Convertisseur abaisseur (Buck) ; Convertisseur survolteur (Boost); ADRC; ESO; ADRC basé sur l'erreur;Commande en cascade; PI.

Acknowledgment

First and foremost, I would also like to express my deep gratitude to my family for their unconditional love, patience, and unwavering support throughout my academic journey.
I would also like to express my sincere gratitude to my supervisor, Pr. **Belkheiri Mohammed**, for their continuous support, valuable guidance, and insightful feedback throughout the course of this work. Their expertise and encouragement played a vital role in shaping this thesis. I also extend my heartfelt thanks to my co-supervisor, MCB. **Benmiloud Mohammed**, for their availability, constructive remarks, and generous assistance in both technical and practical aspects of the research. My sincere gratitude also goes to Dr. **Khaled Ameur** for their support and help during the experimental part of this study.My appreciation goes to the honorable members of the jury: the president, Pr. **Hadjaissa Aboubakeur**, and the examiner, MCB. **Rahmani belkacem**, for accepting to evaluate my work and for their time and valuable comments which contributed to enriching this thesis.Finally, I would like to thank all the professors, colleagues, and staff members who, directly or indirectly, contributed to the successful completion of this project. I would also like to sincerely thank the **l'Aboratoire d'Analyse et de Commande des Systémes d'Energie et Réseaux électrique (LACoSERE)** and the **Telecommunication Signals and Systems (LTSS)** for providing the technical environment, resources, and support.
This work marks a significant step in my academic journey, and I hope it serves as a foundation for future research and practical contributions in the field of control systems and power electronics.

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General Introduction

Industrial applications require precise, stable, and efficient machines for automation and manufacturing tasks. Control engineering is crucial for designing and implementing dynamic systems. Three main categories of control systems are logic-based control, advanced control, and classical control. Classical control techniques like proportional-integral-derivative (PID) controllers are popular but face limitations due to technology advancements. Advanced control methods like Active Disturbance Rejection Control (ADRC) are promising for managing uncertainties and rejecting disturbances in real time.

Han was the first to propose active disturbance rejection control (ADRC) in 1998. Despite the fact that theoretical justification was lagging behind for a while, ADRC has grown to be quite appealing to applied researchers. This is because its innovative ideas, straightforward engineering implementation, and exceptional performance were quickly converted into something useful in engineering practice: the capacity to handle a wide range of uncertainties, excellent transient response, easy implementation, and energy savings, to mention a few. Almost every area of control engineering appears to be covered by the wide range of applications, including motion control, web tension regulation, DC–DC power converter, chemical processes, micro-electromechanical systems gyroscope, speed control of induction motors, and permanent-magnet synchronous motors,brushless DC servo low-velocity compensation, ALSTOM gasifier benchmark problem, boiler–turbine–generator control systems, and fractional-order system [1].

Designing and implementing ADRC for DC/DC converters applications is the aim of this study. Understanding the theoretical underpinnings of ADRC, contrasting it with conventional control techniques, and assessing its effectiveness through simulation and experimental validation will be the main goals of this work. Our goal is to show how ADRC may effectively reject disturbances, improve dynamic response, and increase system robustness by integrating it into a DC/DC converter.
Overall, our brief consists of four chapters:

- **Chapter 1**: offers an overview of control systems, mutant in mind classical and advanced control methods, with detailed discussion on ADRC.
- **Chapter 2**: Defines the theoretical basis of DC/DC converter.
- **Chapter 3**: Simulation of DC/DC converter controlled by ADRC with comparison Buck-converter with PI controller.
- **Chapter 4**: Experimental validation of Buck-converter controlled by ADRC .

Chapter 1

Overview on ADRC

1.1 Introduction

In contemporary engineering, control systems are essential for the precise and stable operation of machinery, processes, and dynamic systems. Control systems are crucial for managing variables like voltage, speed, temperature, and pressure in a variety of applications, including robotics, power electronics, industrial automation, and aerospace. Designing controllers that optimize performance, correct for disruptions, and guarantee desired system behavior is the main goal of control engineering. To address the increasing complexity of engineering systems, a variety of control mechanisms have been developed over time. Mathematical techniques like proportional-integral-derivative (PID) controllers, which are still extensively used because of their simplicity and efficacy, are the foundation of early approaches, such as classical control systems. However, nonlinearities, parameter changes, and external disturbances all of which are prevalent in real-world applications often provide challenges for these conventional approaches. Researchers have investigated sophisticated management strategies, such as Active Disturbance Rejection control (ADRC), which offers a novel method of managing system uncertainty, in order to overcome these constraints. ADRC is a potent tool for robust control applications because it actively estimates and compensates for disturbances in real time, in contrast to traditional approaches that rely on accurate system modeling. An overview of control system classification is given in this chapter, along with an introduction to ADRC as an advanced control approach and a list of its benefits over traditional techniques, and comparing the performance of ADRC with PI controller. The groundwork for comprehending ADRC's function in power electronics, specifically in DC/DC Buck-converter, will be laid by the conversation.

1.2 Classification of control methods

The distinction between classical, modern, and advanced control systems lies in their methodologies, applications, and theoretical foundations. Classical control primarily utilizes frequency domain techniques, making it suitable for simpler, lower-order systems. In contrast, modern control employs state-space representations, allowing for more complex, multi-input, multi-output systems. Advanced control integrates both

classical and modern approaches, enhancing robustness and optimality in system performance.

A. Classical control methods:
- Utilizes frequency domain methods, such as Bode and Nyquist plots.
- Best suited for single-input single-output systems.
- Focuses on stability and response time, often using PID controllers. [2]

B. Modern control methods:
- Employs state-space approaches, facilitating the analysis of higher-order systems.
- Effective for complex systems with multiple inputs and outputs.
- Includes Linear Quadratic Regulator (LQR) and Model Predictive Control (MPC). [3] [4]

C. Advanced control methods:
- Combines classical and modern techniques to leverage their strengths.
- Aims for optimal performance and robustness in dynamic environments.
- Switched Model Predictive Control (SMPC) demonstrates superior performance in nonlinear process control, and ADRC that we will see it in this research. [5] [6]

1.3 Active disturbance rejection control

An alternative that combines the strength of contemporary model-based techniques with the simplicity of application seen in traditional PID-type control systems is active disturbance rejection control, or ADRC. ADRC's foundation is an observer that treats modeling uncertainties and actual disturbances together, requiring only a very coarse process model to design a control loop. This makes ADRC a desirable option for practitioners and offers good robustness against process variations. Current uses include temperature and tension management, motion control, power electronics, and superconducting radio frequency cavities. In contrast to model-based approaches like model predictive control or embedded model control, which require an explicit model of the process to be controlled, the linear case of ADRC is equivalent to a special case of classical state space control with disturbance estimation and compensation based on the internal model principle.ADRC, on the other hand, does only assume a specific canonical model regardless of the actual dynamics of the process, ADRC treats all modeling errors as disturbances. Naturally, this could result in worse performance as compared to a controller that is based on an accurate process model or a reference trajectory model. [7]
In this chapter we will providing an introduction to the linear case of ADRC, a series of simulative experiments to test the performance of the ADRC when being faced with varying process parameters or structural uncertainties.

1.4 Linear active disturbance rejection control

The objective of this section is to reiterate and present the linear instance of ADRC in a self-contained manner. Since many systems, albeit technically nonlinear and higher-order, exhibit dominating first-order-like behavior, at least in certain operating points, the first-order case will be considered first and explicitly here, despite the fact that most articles introduce ADRC with a second-order process. According to the internal model principle, linear ADRC can be viewed as a specific case of classical state space control with disturbance compensation.the modeling methodology presented in this section is adapted from the work of [7].

1.4.1 Control first order system by ADRC

Consider a simple first-order process $P(s)$:

$$P(s) = \frac{Y(s)}{U(s)} = \frac{k}{Ts+1} \quad \Rightarrow \quad sY(s) \cdot T + Y(s) = Ku(s) \tag{1.1}$$

with k: DC gain, T: time constant.
The time-domain version is:

$$\dot{y}(t) \cdot T + y(t) = Ku(t)$$

We add an input disturbance $d(t)$ to the process and define $b = \frac{K}{T}$:

$$\dot{y}(t) = \frac{1}{T}d(t) - \frac{1}{T}y(t) + \frac{K}{T}u(t) = \frac{1}{T}d(t) - \frac{1}{T}y(t) + b \cdot u(t) \tag{1.2}$$

As the final modeling step, we substitute $b = b_0 + \Delta b$, where:

- $b_0 = \frac{K}{T}$: known part
- Δb: modeling error (unknown)

We now obtain the disturbed first-order model:

$$\dot{y}(t) = \left(-\frac{1}{T}y(t) + \frac{1}{T}d(t) + \Delta b \cdot u(t)\right) + b_0 \cdot u(t) = f(t) + b_0 \cdot u(t) \tag{1.3}$$

A state-space representation is used for estimation:

$$\begin{bmatrix}\dot{x}_1(t)\\ \dot{x}_2(t)\end{bmatrix} = \begin{bmatrix}0 & 1\\ 0 & 0\end{bmatrix}\begin{bmatrix}x_1(t)\\ x_2(t)\end{bmatrix} + \begin{bmatrix}b_0\\ 0\end{bmatrix}u(t) + \begin{bmatrix}0\\ 1\end{bmatrix}\dot{f}(t) \tag{1.4}$$

Output:

$$y(t) = \begin{bmatrix}1 & 0\end{bmatrix}\begin{bmatrix}x_1(t)\\ x_2(t)\end{bmatrix}$$

Obviously, a state observer for this type of process can only be constructed using the input $u(t)$ and the output $y(t)$ of the process, since the "virtual" input $\dot{f}(t)$ cannot be tracked. Equation (1.6) provides the structure of the Extended State Observer (ESO), which is essentially the integrator process expanded by a generalized disturbance. It

should be noted that a Luenberger observer is used in the linear version of Active Disturbance Rejection Control (ADRC). For estimation using a linear observer:

$$\begin{bmatrix}\dot{\hat{x}}_1(t)\\ \dot{\hat{x}}_2(t)\end{bmatrix} = \begin{bmatrix}0 & 1\\ 0 & 0\end{bmatrix}\begin{bmatrix}\hat{x}_1(t)\\ \hat{x}_2(t)\end{bmatrix} + \begin{bmatrix}b_0\\ 0\end{bmatrix} u(t) + \begin{bmatrix}l_1\\ l_2\end{bmatrix}(y(t) - \hat{x}_1(t)) \tag{1.5}$$

$$\begin{bmatrix}-l_1 & 0\\ -l_2 & 1\end{bmatrix}\begin{bmatrix}\hat{x}_1(t)\\ \hat{x}_2(t)\end{bmatrix} + \begin{bmatrix}b_0\\ 0\end{bmatrix} u(t) + \begin{bmatrix}l_1\\ l_2\end{bmatrix} y(t) \tag{1.6}$$

Let:

$$\hat{x}_1(t) = y(t), \quad \hat{x}_2(t) = \hat{f}(t)$$

The final control law becomes:

$$u(t) = \frac{u_0(t) - \hat{f}(t)}{b_0} \quad \text{with} \quad u_0(t) = k_p\,(r(t) - \hat{y}(t)) \tag{1.7}$$

Figure 1. shows the control loop's corresponding structure. Although we do have an estimation-based state feedback controller because Kp acts on y(t) rather than the actual output y(t), practitioners will notice the striking similarities to a classical proportional controller. The output of a linear proportional controller is denoted by u0(t) in Equation (1.7). The remaining control rule in u(t) is selected so that, in the event that

$$\hat{f}(t) \approx f(t)$$

the linear controller acts on a normalized integrator process. By inserting Equation (1.7) into Equation (1.2), the effect is visible:

$$\dot{y}(t) = f(t) + b_0 \cdot \frac{u_0(t) - \hat{f}(t)}{b_0} = (f(t) - \hat{f}(t)) + u_0(t) \approx u_0(t) = k_p \cdot (r(t) - \hat{y}(t)) \tag{1.8}$$

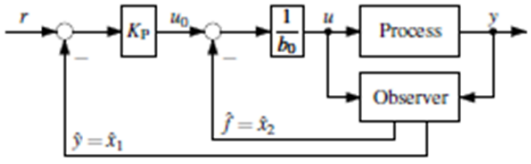


Figure 1.1: control loop structure with ADRC for a first-order process.

We obtain a first-order closed-loop behavior with a pole, $S^{CL} = -K_P$, when $\hat{y}(t) = y(t)$:

$$\frac{1}{k_p}\dot{y}(t) + \hat{y}(t) \approx \frac{1}{k_p}\dot{y}(t) + y(t) = r(t) \tag{1.9}$$

• No matter the parameters of the real process, one only needs to build a proportional controller once to achieve the same closed loop behavior if the state estimator and disturbance rejection function correctly. For instance, a desired first-order system with a 2% settling time can be used to compute KP.

$$K_P \approx \frac{4}{T_{\text{settle}}}$$

To choose observer poles, we place both observer poles (eigenvalues of the ESO matrix $A - LC$) at a negative real value, called S_{ESO}. They are purposefully made quicker than the controller's pole:

$$S_{\text{ESO}} = \text{Factor} \cdot S_{\text{CL}} = \text{Factor} \cdot (-k_p)$$

Typical Factor range: $\text{Factor} = 3 \dots 10$

• "Bandwidth parameterization" is another term for placing all observer poles at a single point. We can calculate the required observer gains for the common pole position S_{ESO} from its characteristic polynomial, since the observer's error dynamics are determined by the matrix $A - LC$:

$$\det(sI - (A - LC)) = s^2 + l_1 s + l_2 = (s - S_{\text{ESO}})^2 = s^2 - 2S_{\text{ESO}} s + S_{\text{ESO}}^2 \tag{1.10}$$

From this equation, the solutions for l_1 and l_2 are:

$$l_1 = -2S_{\text{ESO}}, \quad l_2 = S_{\text{ESO}}^2 \tag{1.11}$$

1.4.2 Simulative experiments

In practice, constraints such as limited observer speed and actuator saturation necessitate careful tuning, but in theory ADRC can perfectly reject disturbances and handle parameter variations if measurements and actuators are ideal. This section uses MATLAB/Simulink simulations to investigate how well ADRC performs under these practical limitations.

First-Order ADRC with a First-Order Process

To evaluate ADRC's performance in real-life situations, including dead time, actuator limitations, disturbances, and parameter changes, a series of simulations are conducted to assess its robustness, tracking accuracy, and disturbance rejection capability under varying operating conditions. Consider the first-order system:

$$P(s) = \frac{K}{Ts + 1}$$

with $K = 1$, $T = 1$

- Settling time: $T_{\text{SETTLE}} = 1 \Rightarrow K_P = 4$
- Estimated system gain: $b_0 = \frac{K}{T} = 1$
- Observer pole location: $S_{\text{ESO}} = 10 \cdot S_{\text{CL}} = -40$
- Observer gains are obtained via Equation(1.11)

1. **Sensitivity to Process Parameter Variations**

   in this effect we only change the parameters of the system without change the ADRC parameters : $b_0 = K/T = 1$, $T_{\text{settle}} = 1$, $s^{\text{ESO}} = 10 \cdot s^{\text{CL}}$.

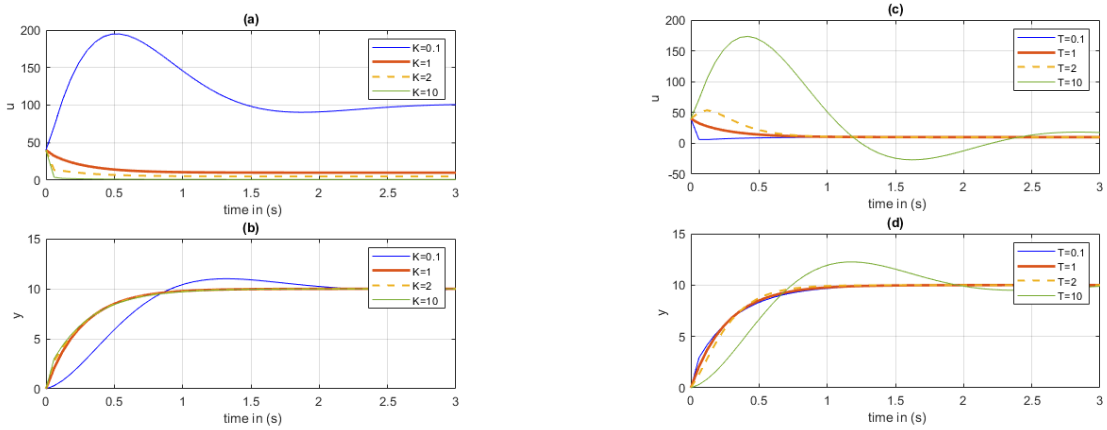


Figure 1.2: variation of K ;closed loop step response(b) with controller output (a). variation of T;closed loop step response(d) with controller output (c).

Simulation Results and Performance Analysis

The ADRC scheme exhibits a good robustness against the plant gain K and time constant T variation (up to a factor of 10), tracking performance of the system is still good. With significant parameter changes, only mild overshoots or settling delays can be noticed.

2. **Effect of Observer Pole Locations (Speed of ESO)**

The impact of the observer pole positions on the overall system performance is examined in this case. In order to investigate the trade-off between quick disturbance estimation and noise sensitivity, several observer speeds are investigated by altering the observer bandwidth.

Simulation Results and Performance Analysis

Smaller ESO scale rate leads to better disturbance estimation andfaster response.A larger sESO ($s^{\mathrm{ESO}} = 100 \cdot s^{\mathrm{CL}}$) makes the system more responsive, but also sensitive to noise.Performance and robustness are well-balanced at a modest observer speed.the result will shown in Fig 1.3

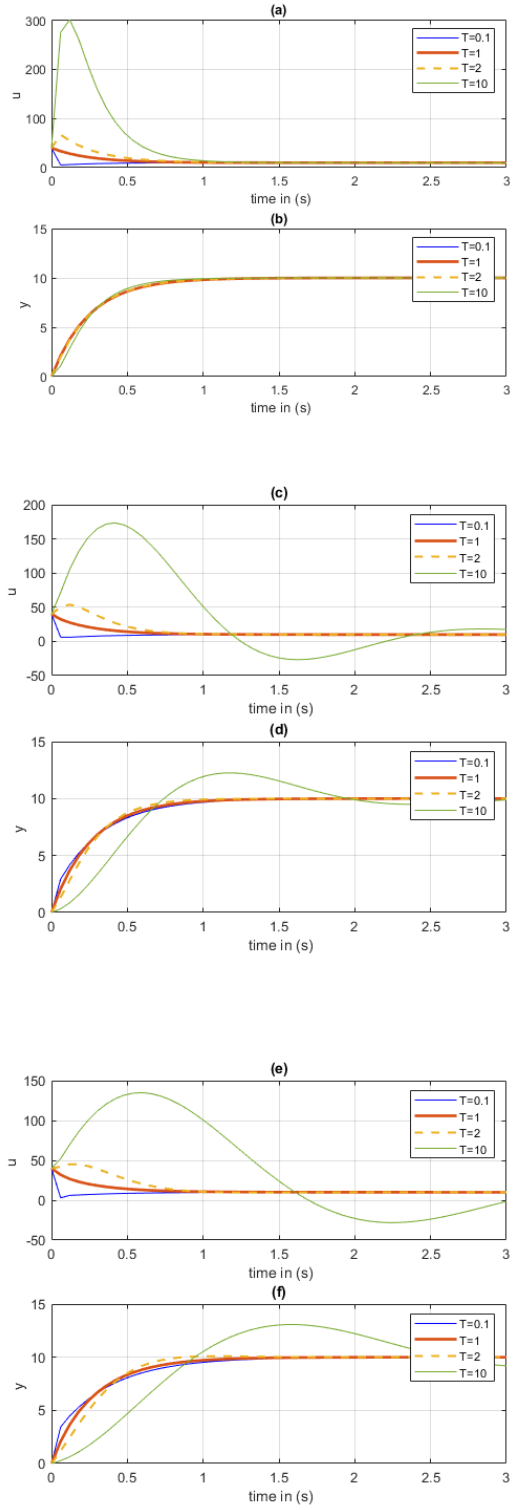


Figure 1.3: influence of observer poles under variation of time constant.(a) controller output ,$s^{\mathrm{ESO}} = 100 \cdot s^{\mathrm{CL}}$ with closed loop step response(b); (c) controller output,$s^{\mathrm{ESO}} = 10 \cdot s^{\mathrm{CL}}$ with closed loop step response(d);(e) controller output, $s^{\mathrm{ESO}} = 5 \cdot s^{\mathrm{CL}}$ with closed loop step response(f).

3. **Effect of Actuator Saturation**

In this part, actuator saturation is introduced to observe how the ADRC controller performs under control signal constraints. Simulations are carried out with limited control input, and different values of tuning parameters K and T are tested to evaluate the controller's effectiveness in maintaining output performance.

Simulation Results and Performance Analysis

In the first example, when the saturation bound $|u_{\text{lim}}| \leq 5$ and the reference is 10, the system is able to follow the reference well when K = 10,but the control effort is now small since the high gain results in less control effort needed.
In the second case, even if we demanded that only T be increased (with the same saturation and reference =10), the system will not achieve the reference due to lack of control energy — the actuator has a limit and cannot supply sufficient input. In the third situation, the output successfully tracks the reference when it is decreased to "1" under the same saturation and parameter modifications. In conclusion, when the necessary control signal above the saturation limit, tracking fails. Higher plant gain or lower reference values aid in maintaining the control effort within the permitted range.the result will shown in Fig 1.4

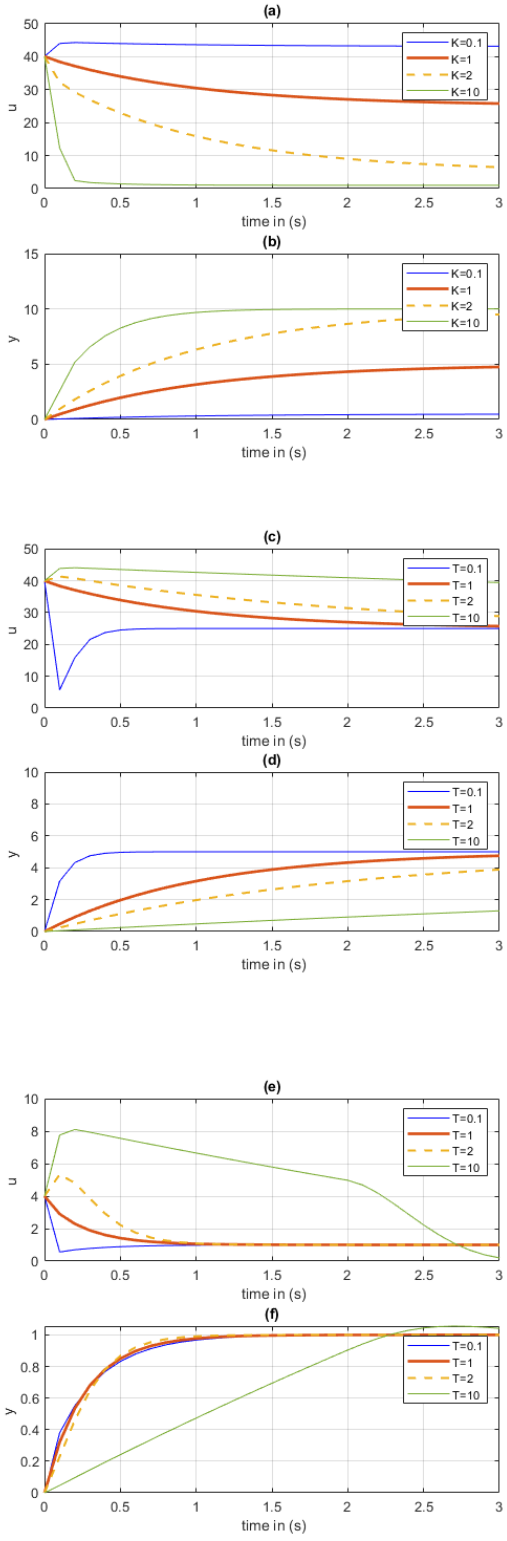


Figure 1.4: ADRC response under Actuator saturation constraints.

4. **Comparison to PI Control**

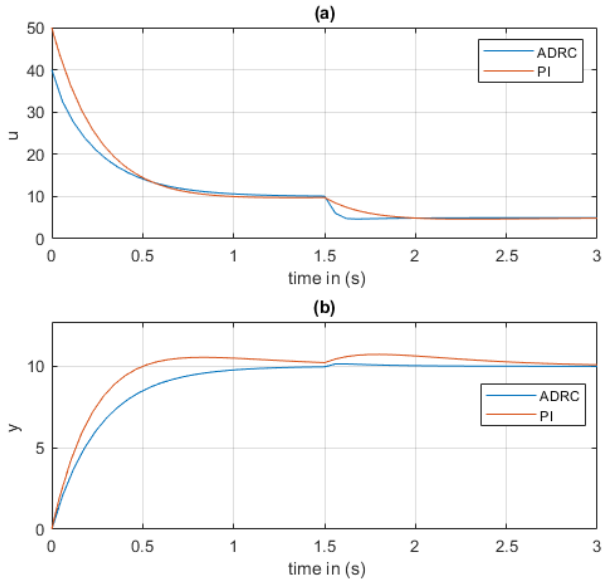


Figure 1.5: Comparison of ADRC and PI Controllers under Model Uncertainty

Simulation Results and Performance Analysis

Both ADRC and PI controllers exhibit respectable tracking performance under nominal conditions (K=1,T=1). Although the PI controller reacts faster, it consumes a greater initial control effort and adds a small overshoot. The ADRC controller maintains strong stability and accomplishes smoother control without overshoot prior to the disturbance. A step disturbance is added to the controller input at t=1,5s. This results in a brief overshoot that is seen in the control signals (subplot a) and outputs (subplot b). Although ADRC reacts a little more slowly than PI, both controllers are able to reject the disturbance and go back to the reference.

1.5 Conclusion

The simulation results confirm that the Active Disturbance Rejection Control (ADRC) strategy offers excellent robustness against plant parameter variations, including changes in system gain K and time constant T . Even with a tenfold change in parameters, the system maintains satisfactory tracking performance, with only minor overshoot or settling time increase. The effectiveness of the extended state observer (ESO) is shown to depend on its tuning; while a faster observer improves responsiveness, it may amplify measurement noise, highlighting the importance of balancing observer speed and noise sensitivity.
Furthermore, actuator saturation plays a critical role in system performance. When the required control effort exceeds the saturation limits, the reference cannot be tracked

accurately. However, increasing the plant gain or reducing the reference value helps keep the control signal within limits, thereby maintaining performance.
In comparison to a PI controller, ADRC provides smoother output tracking with less overshoot and better disturbance rejection, though it responds slightly more slowly. These results demonstrate ADRC's superior robustness and stability, especially under parameter uncertainties and external disturbances, making it a compelling control strategy for DC/DC converters.

Chapter 2

Modelling of DC/DC converters

2.1 Introduction

DC/DC converters are a key building block of modern power electronic systems, particularly in renewable energy applications like photovoltaic and battery-powered systems. Their primary job is to convert an input voltage to an output voltage level with as much efficiency as they can manage and as reliably as possible. The chapter provides a general concept of DC/DC conversion: An overview of common converters topologies specially Buck-converter. therefore will be used as the objective of the Active Disturbance Rejection Control (ADRC) here.

2.2 Overview of DC/DC Converters

DC/DC converters are electronic circuits used to convert one level of DC voltage into another, enabling efficient power management in a wide range of applications. These converters are broadly categorized into non-isolated and isolated types. Non-isolated converters, such as Buck, Boost, and Buck-Boost, are commonly used when electrical isolation is not required and are favored for their simplicity and high efficiency. In contrast, isolated converters, like Flyback, Forward, and Full-Bridge topologies, use a transformer to provide galvanic isolation between the input and output, making them suitable for applications where safety and ground separation are essential. Both types play a critical role in modern power systems, from consumer electronics to industrial and renewable energy systems.

2.3 Step-Down: Buck-converter

2.3.1 Overview of Buck-converter

A DC/DC step-down converter that lowers the input voltage to a lower output voltage is called a Buck converter. An inductor and capacitor are used to smooth the output after a transistor (often a MOSFET) is turned on and off at a high frequency. [8]

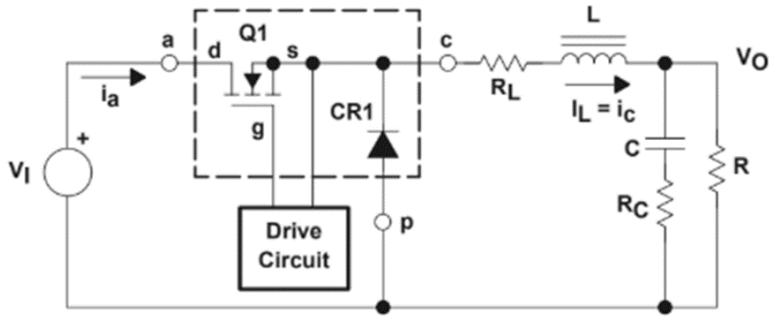


Figure 2.1: Buck power stage schematic

The components used in the DC/DC converter circuit are as follows:

- **Input voltage:** V_{I}
- **Switch:** MOSFET ($Q1$)
- **Diode:** $CR1$ (freewheeling)
- **Inductor:** $L(H)$
- **Capacitor:** $C(F)$
- **Load:** R (Ω)

Q1 is frequently turned on and off during regular buck power stage operation, with the control circuit controlling the on and off periods. The L/C output filter filters the train of pulses created by this switching operation at the intersection of Q1, CR1, and L to provide the dc output voltage, or V_o. A more thorough quantitative analysis can be found in the parts that follow. [9]

2.3.2 Buck Steady-State Continuous Conduction Mode Analysis

The steady-state operation in continuous conduction mode is described as follows. A derivation of the voltage conversion relationship for the continuous conduction mode buck power stage is the primary output of this section. This result is significant because it demonstrates how input voltage and duty cycle affect output voltage or, in the other case, how input voltage and output voltage may be used to determine duty cycle. A steady-state system is one in which the duty-cycle, output load current, input voltage, and output voltage are all constant. In order to denote a steady-state quantity, variable names are typically capitalized. The Buck power stage assumes two states every switching cycle when operating in continuous conduction mode. When CR1 is OFF and Q1 is ON, this is known as the ON state.When CR1 is ON and Q1 is OFF, this is known as the OFF state. Each of the two states can be represented by a straightforward linear circuit in which the switches are swapped out for their corresponding circuits in each state.The circuit diagram for each of the two states is

shown in Figure 2.2. [9]
The output voltage of a Buck converter can be expressed as

$$V_o = \frac{T_{\mathrm{ON}}}{T_s} \cdot V_i = d \cdot V_i$$

This relation is valid under the following condition:

$$V_i > V_o$$

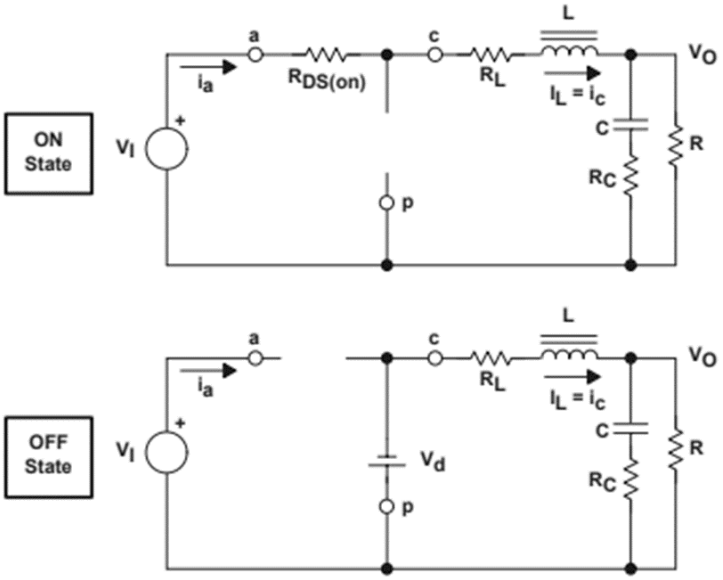


Figure 2.2: Buck-converter states

The ON state lasts for $D \cdot T_S = T_{\mathrm{ON}}$, where D is the duty cycle, which is determined by the control circuit and is represented as the ratio of the switch's ON time to its whole switching cycle duration, T_S. T_{OFF} stands for the duration of the OFF state. T_{OFF} is equal to $(1-D) \cdot T_S$, since continuous mode only has two states every switching cycle. D' is another name for the number $(1 - D)$. These times are shown along with the waveforms in Figure 2.3. [9]

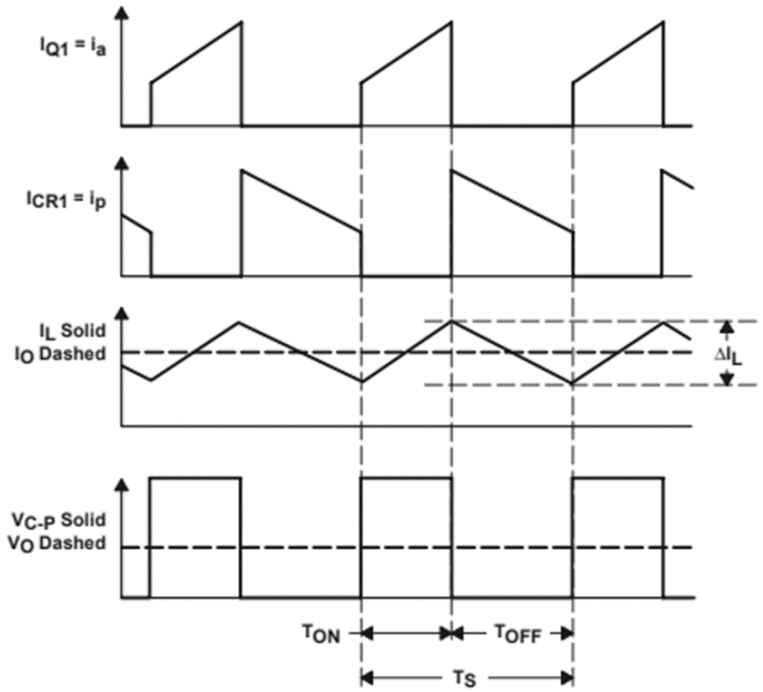


Figure 2.3: Continuous-Mode Buck-converter stage waveforms

Mode 1: Switch ON (S is closed)
When the switch S is closed:

- The diode is reverse biased.
- The input voltage V_{in} supplies power to both the load and the inductor.
- The inductor stores energy.

The voltage across the inductor is:

$$V_L = V_{\text{in}} - V_o \tag{2.1}$$

The rate of change of inductor current is:

$$\frac{di_L}{dt} = \frac{V_{\text{in}} - V_o}{L} \tag{2.2}$$

Mode 2: Switch OFF (S is open)
When the switch S is open:

- The diode becomes forward biased.
- The inductor releases stored energy into the load.

The voltage across the inductor is:

$$V_L = -V_o \tag{2.3}$$

The rate of change of inductor current is:

$$\frac{di_L}{dt} = -\frac{V_o}{L} \tag{2.4}$$

2.3.3 Averaged state-space Model of Buck converter in (CCM)

1. State variables:

   - $x_1 = i_L$: Inductor current
   - $x_2 = V_o$: Output voltage (capacitor voltage)
   - Control input: $d(t)$: Duty cycle

2. State-Space Equations:

Assuming ideal switching and continuous conduction mode (CCM), the system can be modeled as follows:

$$\frac{d}{dt}\begin{bmatrix} i_L \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}\begin{bmatrix} i_L \\ V_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_{\text{in}} \cdot d(t) \tag{2.5}$$

The output equation is:

$$y = \begin{bmatrix} 0 & 1 \end{bmatrix}\begin{bmatrix} i_L \\ V_o \end{bmatrix} = V_o \tag{2.6}$$

2.3.4 Switching behavior of Buck converter (PWM control)

A PWM (Pulse Width Modulation) signal is used to control the MOSFET switch. The duration for which the switch remains ON during each switching period T_s is determined by the duty cycle d, where:

$$d \in [0, 1]$$

- Switching Times
- **ON time:** $d \cdot T_s$
- **OFF time:** $(1 - d) \cdot T_s$

In the ideal case, the average output voltage is given by:

$$V_o = d \cdot V_{\text{in}}$$

2.4 Step-up:Boost-converter

2.4.1 Overview of boost converter

A DC/DC step-up converter is called a boost converter. It uses a controlled switch and energy storage components (capacitor and inducer) to raise the input voltage to a higher output voltage. [8]

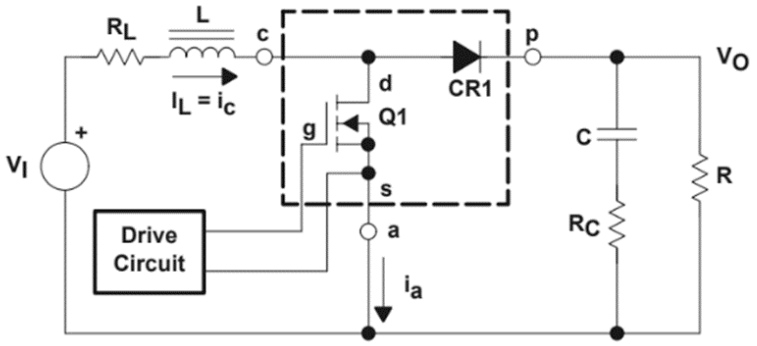


Figure 2.4: Boost power stage schematic

Q1 is frequently turned on and off during regular boost power stage operation, with the control circuit controlling the on and off periods. A train of pulses is produced at the intersection of Q1, CR1, and L by this switching action. An efficient L/C output filter is created even if inductor L is only linked to output capacitor C when CR1 conducts. It generates a dc output voltage, VO, by filtering the pulse train. A more thorough quantitative analysis is provided in the sections that follow. [10]

2.4.2 Boost Steady-State Continuous Conduction Mode Analysis

The steady-state operation in continuous conduction mode is described as follows. A derivation of the voltage conversion relationship for the continuous conduction mode boost power stage is the primary output of this section. This result is significant because it demonstrates how input voltage and duty cycle affect output voltage or, in the opposite direction, how input and output voltages may be used to determine duty cycle. In a steady state, the duty-cycle, output load current, input voltage, and output voltage are all fixed and unchanging. In order to denote a steady-state quantity, variable names are typically capitalized. The boost power stage assumes two states every switching cycle when operating in continuous conduction mode. Q1 is on and CR1 is off while the state is on. Q1 is off while CR1 is on in the off state. Each of the two states can be represented by a straightforward linear circuit in which the switches are swapped out for their corresponding circuit in each state. The linear circuit schematic for each of the two states is displayed in Figure 2.5. [10]

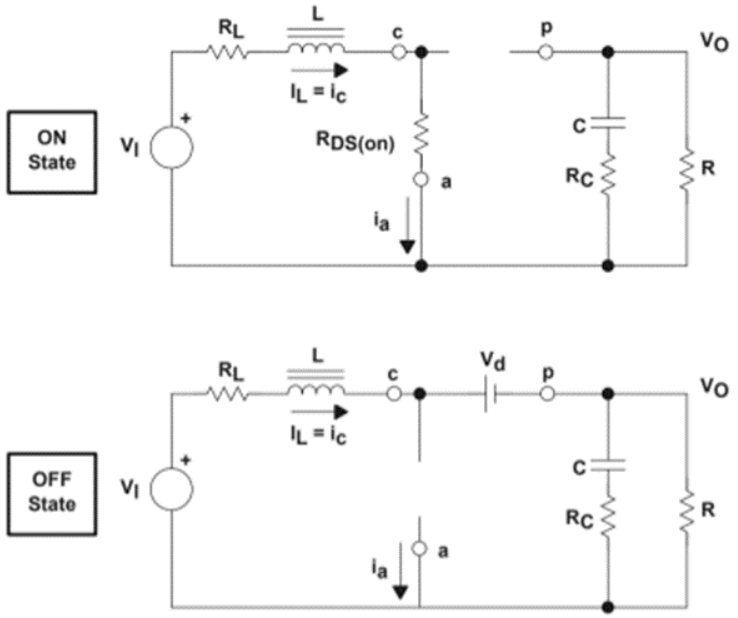


Figure 2.5: Boost power stage states

The duty cycle established by the control circuit, represented as a ratio of the switch on time to the time of one full switching cycle, Ts, is D × TS = TON. This represents the length of the on state. TOFF is the duration of the off state. TOFF is equal to (1–D) × TS because continuous conduction mode only has two states every switching cycle. D' is another name for the number (1–D). Figure 2.5 displays these timings in addition to the waveforms. [10]

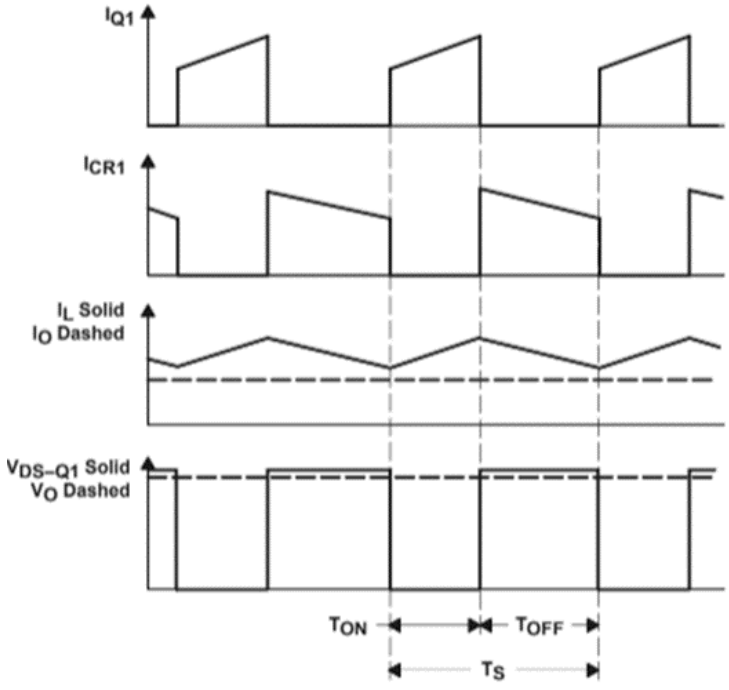


Figure 2.6: Continuous-Mode Boost-converter stage waveforms

When switch S_1 is closed: The system dynamics in this mode are:

$$\begin{cases} \dfrac{di_L}{dt} = \dfrac{V_{\text{in}}}{L} \\ \dfrac{dV_o}{dt} = -\dfrac{V_o}{RC} \end{cases} \tag{2.1}$$

When S_1 is opened: The system dynamics in this mode are:

$$\begin{cases} \dfrac{di_L}{dt} = \dfrac{V_{\text{in}} - V_o}{L} \\ \dfrac{dV_o}{dt} = \dfrac{i_L - \frac{V_o}{R}}{C} \end{cases} \tag{2.2}$$

The average output voltage V_o of a Boost converter in Continuous Conduction Mode (CCM) is given by:

$$V_o = \frac{1}{1-d} \cdot V_{\text{in}} \tag{2.3}$$

This equation is valid under the condition:

$$V_{\text{in}} < V_o$$

where:

- V_o: Output voltage
- V_{in}: Input voltage
- $d \in [0, 1)$: Duty cycle of the PWM signal

2.4.3 Averaged state-space Model of Boost-converter in (CCM)

1. State Variables:
   - $x_1 = i_L$: Inductor current
   - $x_2 = V_o$: Output voltage (capacitor voltage)
   - Control input: $d(t) \in [0, 1]$: Duty cycle
2. Nonlinear State-Space Equations:

   The state-space representation of the Boost converter (in continuous conduction mode) is given by:

$$\frac{d}{dt}\begin{bmatrix} i_L \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1-d(t)}{L} \\ \frac{1-d(t)}{C} & -\frac{1}{RC} \end{bmatrix}\begin{bmatrix} i_L \\ V_o \end{bmatrix} + \begin{bmatrix} \frac{V_{\text{in}}}{L} \\ 0 \end{bmatrix} \tag{2.4}$$

   The output equation is:

$$y = \begin{bmatrix} 0 & 1 \end{bmatrix}\begin{bmatrix} i_L \\ V_o \end{bmatrix} = V_o \tag{2.5}$$

3. Remarks:

- The system is nonlinear due to the presence of $d(t)$ multiplying the state variables.

2.4.4 Switching behavior of Boost-converter (PWM control)

Controlled using a PWM signal. Duty cycle $d \in [0, 1]$ determines how long the switch is ON per switching period T_s.

The ideal output voltage is:

$$V_O = \frac{V_{\text{in}}}{1 - d} \tag{2.6}$$

The output voltage increases as d approaches 1, but component stress and control complexity both increase.

2.5 Conclusion

DC/DC converters are essential components in power electronics, enabling efficient voltage regulation and conversion for various applications. The Buck and Boost topologies represent the most fundamental forms of step-down and step-up converters, respectively. Through proper switching control and energy storage in passive elements (inductors and capacitors), these converters achieve high efficiency and flexible output regulation. Their behavior can be accurately described using averaged and state-space models, which form the basis for control design and system analysis. Understanding their operation and mathematical modeling is crucial for implementing advanced control techniques like ADRC, ensuring both performance and robustness in practical power systems.

Chapter 3

ADRC control of DC/DC converter

3.1 Intoduction

DC/DC converters are widely used in power electronics to regulate voltage level efficiently and ensure effective energy transfer within electrical systems. However, controlling these converters with stability and robustness can be challenging due to their inherent nonlinearity and sensitivity to load variations and input voltage fluctuations. Among modern control strategies, Active Disturbance Rejection Control (ADRC) has proven to be a powerful tool, offering strong disturbance rejection capabilities and robust performance even when the system model is uncertain or incomplete. This chapter focuses on the simulation of DC/DC converters using MATLAB/Simulink, with the goal of comparing the performance of a classical PI controller against that of an ADRC-based controller. The objective is to design a controller capable of estimating and rejecting both internal and external disturbances in real time, while ensuring fast and accurate voltage regulation. Through simulation results, the effectiveness of ADRC in handling the dynamic behavior of the Buck converter is analyzed and compared with the conventional PI approach.

3.2 ADRC-based Control of Buck Converter

In this section, the ADRC is utilized to control the buck converter, the objective being robust voltage regulation in the presence of load disturbances and uncertainty in the system model. It comprises of modeling Buck converter, also designing a controller in two methods that we will see them in this title, simulation of the system under study in MATLAB/SIMULINK and analysis of the simulation findings achieved.
The averaged state-space model (3.1) of a DC/DC Buck converter is a linear second-order system, can be expressed as:

$$\begin{aligned} \dot{x}_1 &= \frac{1}{C}(x_2 - \frac{x_1}{R}) + d_s(t) \\ \dot{x}_2 &= \frac{V_{\text{in}}}{L}(d + d_s(t)) - \frac{x_1}{L} \end{aligned} \tag{3.1}$$

the system has both **matched** and **unmatched uncertainties**, depending on where the control input enters.

the voltage equation: is unmatched uncertainty.
the current equation: is matched uncertainty.

Where:

- x_1: the output voltage V_o
- x_2: the inductor current i_L
- V_{in}: the input voltage
- d: the duty cycle (control input)
- $d_s(t)$: the disturbance or unknown part of the system

in this chapter,the Buck converter is modeled using the following component values:

Table 3.1: Physical Parameters of the Buck Converter

Symbol	**Value**	**Unit**	**Description**
R	50	Ω	Load resistance
L	10	mH	Inductor
C	1	mF	Output capacitor
f_{sw}	10	KHz	Switching Frequency
V_{in}	24	v	Input voltage

These values are adopted from a reference study presented in [11].

Controller design method

3.2.1 Cascade Control for Buck-converter

This study develops inner-loop current controller and outer-loop voltage controller based on ADRC for the average model of the DC/DC buck converter defined by model (3.1). It has two-channel control, control feedback, and interference suppression as features. To increase the system's speed, ESO can be used to predict input voltage and load fluctuations beforehand. These fluctuations can then be removed using a disturbance suppression loop. The ESO obtains the capacitive voltage signal and the inductive current signal, respectively, which are employed as the feedback quantities of the voltage outer loop and the current inner loop.

1. **Design of voltage controller:**

   The voltage controller is designed from the following equation:

$$\frac{dV_O}{dt} = \frac{i_L}{C} - \frac{V_O}{CR} + d_s(t) \tag{3.2}$$

   Let $V_O = y_1$, and $u_1 = i_L$, then:

$$\dot{y}_1 = \frac{1}{C}u_1 - \frac{V_O}{CR} + d_s(t) = b_1 u_1 + f_1(y_1, u_1) \tag{3.3}$$

Where:

- $b_1 = \frac{1}{C}$ is the input gain,
- y_1 is the output (voltage),
- u_1 is the input (inductor current),
- $f_1 = -\frac{V_O}{CR} + d_(t)$ is the total disturbance.

Let $x_1 = y_1$, $x_2 = f_1$, then the system can be rewritten as:

$$\begin{cases} \dot{x} = A_1 x + B_1 u_1 + E_1 \dot{f}_1 \\ y_1 = C_1 x \end{cases} \tag{3.4}$$

Where:

$$A_1 = \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix}, \quad B_1 = \begin{bmatrix} b_1 \\ 0 \end{bmatrix}, \quad E_1 = \begin{bmatrix} 0 \\ 1 \end{bmatrix}, \quad C_1 = \begin{bmatrix} 1 & 0 \end{bmatrix}, \quad x = \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}$$

Second-order ESO

The Extended State Observer (ESO) is defined as:

$$\begin{cases} \dot{\hat{x}} = A_1 \hat{x} + B_1 u_1 + L_{01}(y_1 - \hat{y}_1) \\ \hat{y}_1 = C_1 \hat{x} \end{cases} \tag{3.5}$$

Where:

$$L_{01} = \begin{bmatrix} \beta_{11} \\ \beta_{12} \end{bmatrix}$$

Control Law

Since the system has a relative degree of one, proportional control is sufficient:

$$u = k_1(r_1 - \hat{x}_1) \tag{3.6}$$

Where r_1 is the voltage reference, and k_1 is a proportional gain. Using $\hat{x}_2 = \hat{f}_1$ from the LESO, the final control input is:

$$u_1 = \frac{u - \hat{x}_2}{b_1} = \frac{k_1(r_1 - \hat{x}_1) - \hat{x}_2}{b_1} \tag{3.7}$$

Closed-loop Behavior

From the equation (3.14) into (3.10):

$$\dot{y}_1 = u - \hat{x}_2 + f_1 \approx u \tag{3.8}$$

If $\hat{y}_1(t) \approx y_1(t)$, we obtain a first-order closed-loop system with the pole:

$$s_1^{CL} = -K_1$$

To achieve a 2% settling time T_{settle}, the gain is:

$$K_1 = \frac{4}{T_{\text{settle,voltage}}}$$

ESO Tuning

Choose observer poles as:

$$s_{1,2}^{ESO1} = s^{ESO1} = (3 \dots 10) \cdot s_1^{CL}$$

Then the observer gains are:

$$\beta_{11} = -2s^{ESO1}, \quad \beta_{12} = (s^{ESO1})^2$$

2. **Design of current controller:**

Design the current controller according to the second equation. The current controller is designed as follows:

$$\frac{di_L}{dt} = \frac{V_{\text{in}}}{L}[d + d_s(t)] - \frac{1}{L}V_O \tag{3.9}$$

Let $i_L = y_2$, $d = u_2$, then:

$$\dot{y}_2 = \frac{V_{\text{in}}}{L}u_2 + \frac{V_{\text{in}}}{L}d_s(t) - \frac{1}{L}V_O = b_2u_2 + f_2(y_2, u_2) \tag{3.10}$$

Where: $b_2 = \frac{V_{\text{in}}}{L}$ is the control gain, y_2 is the system output, u_2 is the system input, $f_2 = \frac{V_{\text{in}}}{L}d_s(t) - \frac{1}{L}V_O$ is the total disturbance.

Let $x_1 = y_2$, $x_2 = f_2$, then the system becomes:

$$\begin{cases} \dot{x} = A_2x + B_2u_2 + E_2\dot{f}_2 \\ y_2 = C_2x \end{cases} \tag{3.11}$$

Where:

$$A_2 = \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix}, \quad B_2 = \begin{bmatrix} b_2 \\ 0 \end{bmatrix}, \quad E_2 = \begin{bmatrix} 0 \\ 1 \end{bmatrix}, \quad C_2 = \begin{bmatrix} 1 & 0 \end{bmatrix}, \quad x = \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}$$

Second-order ESO (Extended State Observer)

$$\begin{cases} \dot{\hat{x}} = A_2\hat{x} + B_2u_2 + L_{02}(y_2 - \hat{y}_2) \\ \hat{y}_2 = C_2\hat{x} \end{cases} \tag{3.12}$$

Where the observer gain vector is:

$$L_{02} = \begin{bmatrix} \beta_{21} \\ \beta_{22} \end{bmatrix}$$

Control Law

According to the equation(3.2), the relative degree is 1. So, proportional control is used:

$$u' = k_2(r_2 - \hat{x}_1) \tag{3.13}$$

Here, $\hat{x}_2 = \hat{f}_2$ is estimated by the LESO. To automatically compensate the total disturbance, the final control law is:

$$u_2 = \frac{u' - \hat{x}_2}{b_2} = \frac{k_2(r_2 - \hat{x}_1) - \hat{x}_2}{b_2} \tag{3.14}$$

Where r_2 is the reference input, and k_2 is the proportional gain.

We get from Equation (3.7) in Equation (3.3):

$$\dot{y}_2 = u' - \hat{x}_2 + f_2 \approx u' \tag{3.15}$$

If $\hat{y}_2(t) \approx y_2(t)$, then we obtain a first-order closed-loop behavior with a pole:

$$s_2^{CL} = -K_2$$

ESO Tuning Parameters

To achieve a desired settling time T_{settle} (for 2% error), choose:

$$K_2 = \frac{4}{T_{\text{settle,current}}}$$

Choose observer poles faster than the controller pole:

$$s_{1,2}^{ESO2} = s^{ESO2} = (3 \dots 10) \cdot s_2^{CL}$$

Then, the observer gains are calculated as:

$$\beta_{21} = -2s^{ESO2}, \quad \beta_{22} = (s^{ESO2})^2$$

3.2.2 Simulation Results of cascade control for Buck-converter

In the cascade ADRC controller, two independent loops are implemented:
An outer voltage loop, responsible for regulating the output voltage.
An inner current loop, responsible for tracking the reference current generated by the outer loop.
The ADRC parameters utilized in both loops are maintained consistent throughout all simulation situations for uniformity and an equitable performance comparison. Each loop's design is based on a set settling time target (Tsettle), which establishes the dynamics of the observer and controller.

- for the outer loop , the settling time is:

$$T_{\text{settle,voltage}} = 0.02 \text{ s}$$

The poles of Extanded state observer (ESO) are placed at:

$$s^{ESO1} = (5) \cdot s_1^{CL} = -1000$$

$$\beta_{11} = -2s^{ESO1} = 2000, \quad \beta_{12} = (s^{ESO1})^2 = 1000000$$

- For the current loop, the desired settling time is shorter to ensure a faster dynamic:

$$T_{\text{settle,current}} = (1/10) * T_{\text{settle,voltage}}$$

The ESO of this loop :

$$s^{ESO2} = (5) \cdot s_2^{CL} = -10000$$

$$\beta_{21} = -2s^{ESO2} = 20000, \quad \beta_{22} = (s^{ESO2})^2 = 100000000$$

The controller gains are computed accordingly $b_1 = 1/C$, $b_2 = V_{in}/L$ and remain constant throughout the different test cases to provide a fair performance comparison under:

Case 1: Changes in the reference step
A step adjustment in the reference voltage (12-10 V) was provided at t = 0.2 s while maintaining the input voltage and the resistance of the connected load at their nominal values of 24 V and 50 Ω,respectively.

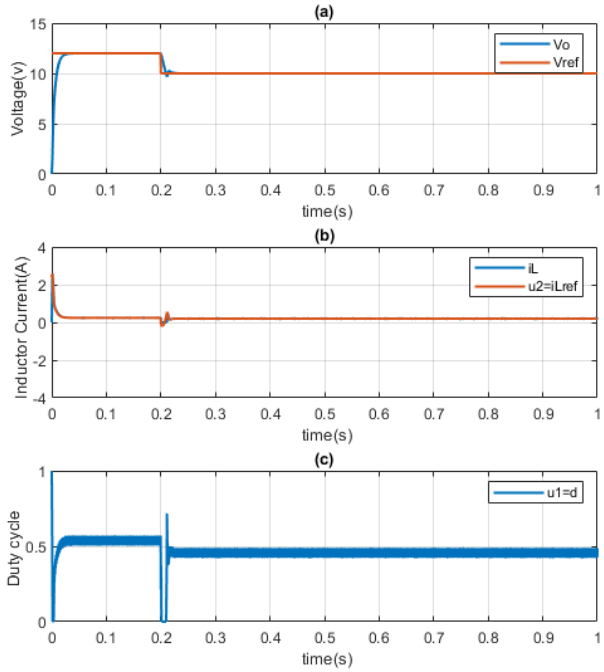


Figure 3.1: system response of cascade control ADRC for Buck-converter (case 1).

Result interpretation:

In the Figure 3.1, a step increase is applied to the voltage reference to evaluate the tracking performance of the cascade ADRC controller.

- The outer loop generates a reference current that corresponds to the new voltage setpoint.
- The inner current loop quickly tracks this new current reference,ensuring that the inductor current changes appropriately to charge the output capacitor and bring the voltage to 10v.
- The output voltage tracks the reference smoothly without any overshooting. this system reaches stability after a settling time of approximately $T_{\text{settle}} = 0.02$ s , when the output remains within a specified tolerance band (typically 2% or 5%) around the reference value.
- Immediately following the reference step, the duty cycle rises, enabling the inductor to store more energy and drive the output voltage to a new value of 10v. The duty cycle stabilizes after the new voltage is attained.

The efficiency of the cascade ADRC structure in controlling voltage reference transitions is demonstrated by the coordinated interaction between the voltage and current loops.

Case 2: Input voltage disturbance.
A step change in input voltage (24–13 V) was introduced at t=0.2s while maintaining a constant connected load resistance of50 Ω with reference 12v.

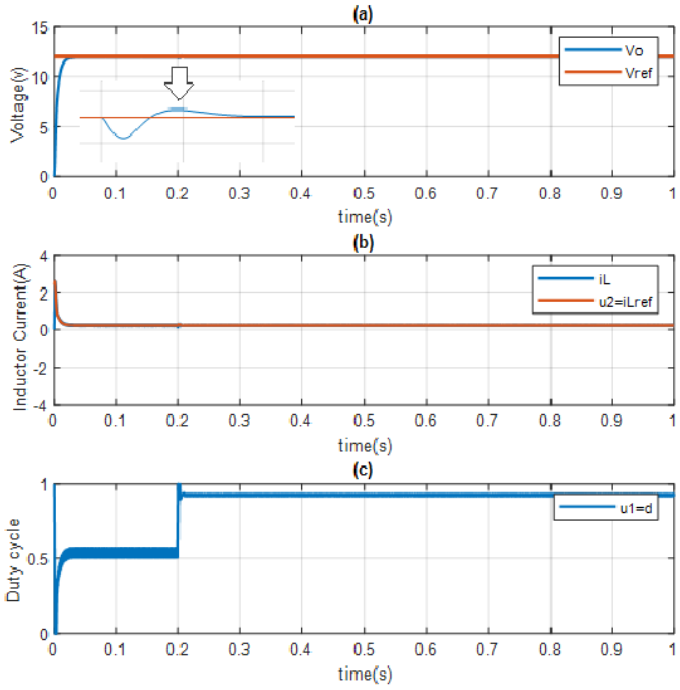


Figure 3.2: system response of cascade control ADRC for Buck-converter (case 2).

Result interpretation:

In this Figure 3.2, the input voltage is suddenly reduced(or increased) to simulate an external power disturbance.

- The outer voltage loop detects the deviation from the desired output voltage and updates the reference current accordingly .
- The inner loop then adjusts the actual inductor current to match the new reference .
- The output voltage experiences a brief deviation but quickly returns to the reference value, demonstrating strong disturbance rejection.
- The duty cycle responds dynamically:
  if the input voltage drops, the controller increases the duty cycle to compensate by allowing the inductor to charge longer. Otherwise if the input voltage rises, the duty cycle decreases accordingly.
- the inductor current tracks the new refrence almost instantly,ensuring stability of the output.

This case highlights how the cascade control structure provides robustness against source-side disturbances through dynamic adjustment of both current and duty ratio.

Case 3: Input voltage disturbances with square wave reference.
In this case, The reference voltage was set as a time-varying square waveform defined by:

$$v_{\text{ref}}(t) = 8 + 4 \cdot \text{square}(2\pi \cdot 0.5 \cdot t)$$

To evaluate the robustness of the controller under input-side disturbances, the input voltage was initially set to 24 V and then decreased to 16 V at $t = 1.7\,\text{s}$. The load resistance and all controller parameters remained unchanged during the test.

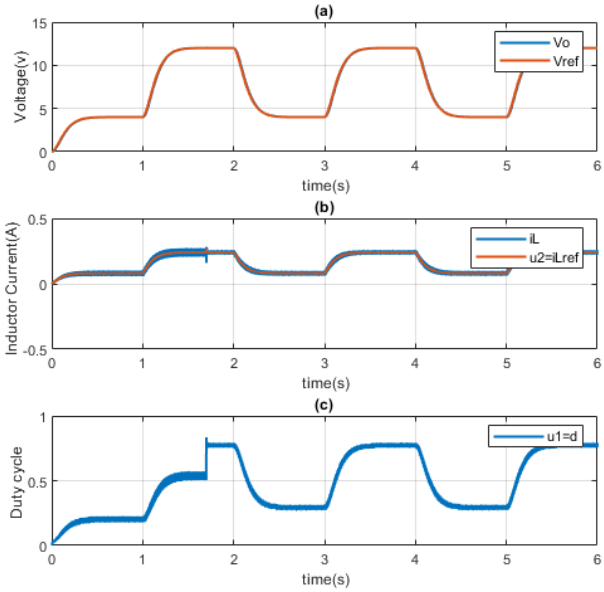


Figure 3.3: system response of cascade control ADRC for Buck-converter in (case 3)

Result interpretation:

The simulation results show that the ADRC-controlled Buck converter successfully tracks the square-wave reference signal, even when subjected to a sudden drop in input voltage. The output voltage follows the desired waveform without overshoot and no steady-state error.

After the disturbance is applied at $t = 1.7\,\text{s}$, the output voltage exhibits a very small transient but quickly returns to tracking the reference signal accurately. This fast recovery demonstrates the effectiveness of the Extended State Observer (ESO) in estimating and compensating for the input disturbance in real time. The duty cycle appears rough due to the fast reaction of the inner current loop, which tightly regulates the inductor current, that becomes sensitive to switching ripple, but more visible variation in the duty cycle.
Overall, the simulation confirms the robustness and stability of the cascade ADRC control strategy under varying reference and supply conditions.

MATLAB/SIMULINK

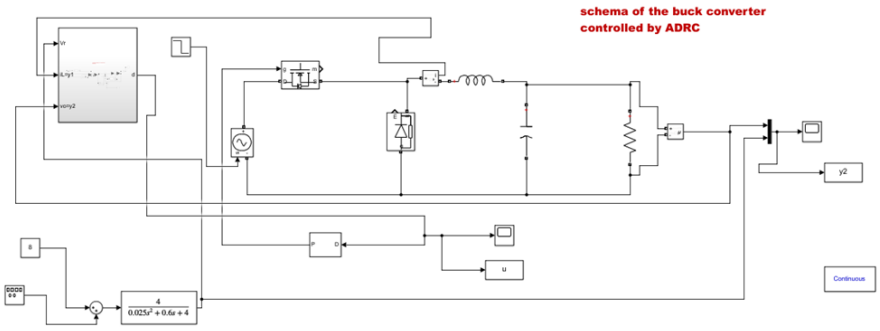


Figure 3.4: Screenshot MATLAB/SIMULINK circuit of Buck-converter by Cascade desing on ADRC.

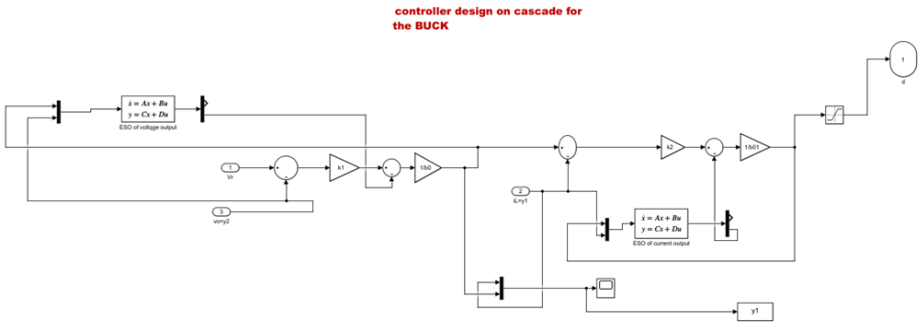


Figure 3.5: Screenshot MATLAB/SIMULINK Blocks of cascade control desing on ADRC for Buck-converter.

3.2.3 Error-based ADRC for Buck-converter

In this method, the ADRC is utilized to control the buck converter. The design is in terms of output error feedback, the objective being robust voltage regulation in the presence of load disturbances and uncertainty in the system model. It comprises of modeling Buck converter, designing of error-based ADRC controller, simulation of the system under study in MATLAB/SIMULINK and analysis of the simulation findings achieved.

Application of the ADRC Principle

Following the ADRC design, from the model (3.1) we get:

$$\frac{d^2V_o}{dt^2} = -\frac{1}{CR}\frac{dV_o}{dt} - \frac{1}{CL}V_o(t) + \frac{V_{in}}{CL}\left[d + d_s(t)\right] \tag{3.16}$$

that: $d = u(t)$ the controller (duty cycle).
In this equation, there are unknown parts such as external disturbance and uncertain parameters. Also, the gain of the system is:

$$b = b_0 + \Delta b$$

Where:

- b_0: known part of the gain
- Δb: unknown part of the gain

So, the equation can be written in the approximate form (referred to as the approximate model):

$$\ddot{v}_o = a_1 v_o + a_2 \dot{v}_o + \Delta b\, u + b_0 u + d(t) \tag{3.17}$$

Which can be reformulated as:

$$\ddot{v}_o = F(\cdot) + b_0 u \tag{3.18}$$

Where $F(\cdot)$ is the **generalized disturbance**, including all unknown dynamics and external disturbances.

In the error domain, only the tracking error between the reference voltage and the actual output voltage is used to design the control input:

$$e = v_o - v_{\text{ref}}$$

Definition of Extended State

Define the extended state:

$$\boldsymbol{z} = \begin{bmatrix} z_1 \\ z_2 \\ z_3 \end{bmatrix} \triangleq \begin{bmatrix} e \\ \dot{e} \\ F^* \end{bmatrix} \in D_z, \quad D_z \triangleq \left\{ x \in \mathbb{R}^2 : \|x\| < r_z \right\}$$

Error Dynamics

Let:

$$z_1 = x_1 - v_{\text{ref}}, \quad \dot{z}_1 = \dot{x}_1 - \dot{v}_{\text{ref}} = -\frac{1}{RC} x_1 + \frac{1}{C} x_2 + d(t) - \dot{v}_{\text{ref}}$$

$$\dot{z}_1 = z_2$$

$$\ddot{z}_1 = \dot{x}_2 - \ddot{v}_{\text{ref}} = \frac{1}{C}\left(-\frac{1}{L} x_1 + \frac{V_{\text{in}}}{L}(u + d(t)) \right) + d(t)$$

$$\dot{z}_2 = b_0 u + F(t), \quad \text{where} \quad b_0 = \frac{V_{\text{in}}}{CL}$$

Hence, the state-space error dynamics of ADRC become:

$$\dot{z}_1 = z_2 \tag{3.19}$$

$$\dot{z}_2 = b_0 u + F(t) \tag{3.20}$$

$$\dot{z}_3 = \dot{F}(t) \tag{3.21}$$

This is known as the **matched uncertainty** model.

Extended State Observer (ESO)

Based on the error model, we construct the ESO using the principle:

$$\text{Observer:} \quad \dot{x} = \text{prediction} + \text{correction}$$

ESO equations:

$$\dot{\hat{z}}_1 = \hat{z}_2 + L_1(z_1 - \hat{z}_1) \tag{3.22}$$
$$\dot{\hat{z}}_2 = b_0 u + L_2(z_1 - \hat{z}_1) \tag{3.23}$$
$$\dot{\hat{z}}_3 = L_3(z_1 - \hat{z}_1) \tag{3.24}$$

Matrix form:

$$\begin{bmatrix} \dot{\hat{z}}_1 \\ \dot{\hat{z}}_2 \\ \dot{\hat{z}}_3 \end{bmatrix} = \underbrace{\begin{bmatrix} -L_1 & 1 & 0 \\ -L_2 & 0 & 1 \\ -L_3 & 0 & 0 \end{bmatrix}}_{A-LC} \begin{bmatrix} \hat{z}_1 \\ \hat{z}_2 \\ \hat{z}_3 \end{bmatrix} + \begin{bmatrix} 0 \\ b_0 \\ 0 \end{bmatrix} u + \begin{bmatrix} L_1 \\ L_2 \\ L_3 \end{bmatrix} y$$

Control Law

The state feedback controller using ESO is:

$$u(t) = \frac{u_0 - \hat{f}(t)}{b_0}, \quad \text{with} \quad u_0 = -K_P z_1 - K_D \hat{z}_2 - \hat{z}_3$$

Tuning Controller Gains

To achieve a critically damped second-order closed-loop behavior with 2% settling time T_{settle}, use:

$$s_{1,2}^{CL} = s^{CL} \approx -\frac{6}{T_{\text{settle}}}$$
$$K_P = (s^{CL})^2, \quad K_D = -2s^{CL}$$

ESO Gain Design

Choose the observer poles as:

$$s_{1,2,3}^{ESO} = s^{ESO} \in [3, 10] \cdot s^{CL}$$

The characteristic polynomial of $(A - LC)$ is:

$$\det(sI-(A-LC)) = s^3+L_1s^2+L_2s+L_3 = (s-s^{ESO})^3 = s^3-3s^{ESO}s^2+3(s^{ESO})^2s-(s^{ESO})^3$$

Matching coefficients, the ESO gains are:

$$L_1 = -3s^{ESO}, \quad L_2 = 3(s^{ESO})^2, \quad L_3 = -(s^{ESO})^3$$

3.2.4 Simulation Results of Error-based ADRC for Buck-converter

To verify the performances of the proposed strategy of this method control (Error-based ADRC), simulation tests were designed in Matlab/Simulink. the circuit parameters that were previously shown in Table 3.1, and the ADRC parameters is shown in Table 3.2.to verify the stability of the system under different cases, two cases were designed,as shown in Table 3.3.

Table 3.2: Computed Error-based ADRC parameters for Buck-converter based on $T_{\text{settle}} = 0.02$ s

Parameter	**Expression**	**Value**
s^{cl}	$-6/T_{\text{settle}}$	-300
K_P	s_{cl}^2	90 000
K_D	$-2 \cdot s_{\text{cl}}$	600
s^{ESO}	$5 \cdot s_{\text{cl}}$	-1500
L_1	$-3 \cdot s_{\text{ESO}}$	7500
L_2	$3 \cdot s_{\text{ESO}}^2$	11 250 000
L_3	$-s_{\text{ESO}}^3$	3.375×10^9
b_0	$V_{\text{in}}/(C \cdot L)$	2400000

Table 3.3: Test cases.

Case	**Reference Signal**	**Load R (Ω)**	**Input Voltage (V_{in})**
1	$v_{\text{ref}}(t) = 8 + 4 \cdot \text{square}(2\pi \cdot 0.5 \cdot t)$	50Ω	Constant at 24V
2	$v_{\text{ref}}(t) = 8 + 4 \cdot \text{square}(2\pi \cdot 0.5 \cdot t)$	50Ω	Drops from 24V to 16V at $t = 1.7$ s
3	$v_{\text{ref}} = 12\,V$	50Ω	Drops from 24V to 13V at $t = 0.2$ s
4	Rises from 10V to 12V at $t = 0.6$ s	Drops from 50Ω to 25Ω at $t = 1.4$ s	Drops from 24V to 16V at $t = 1.1$ s

Case 1:

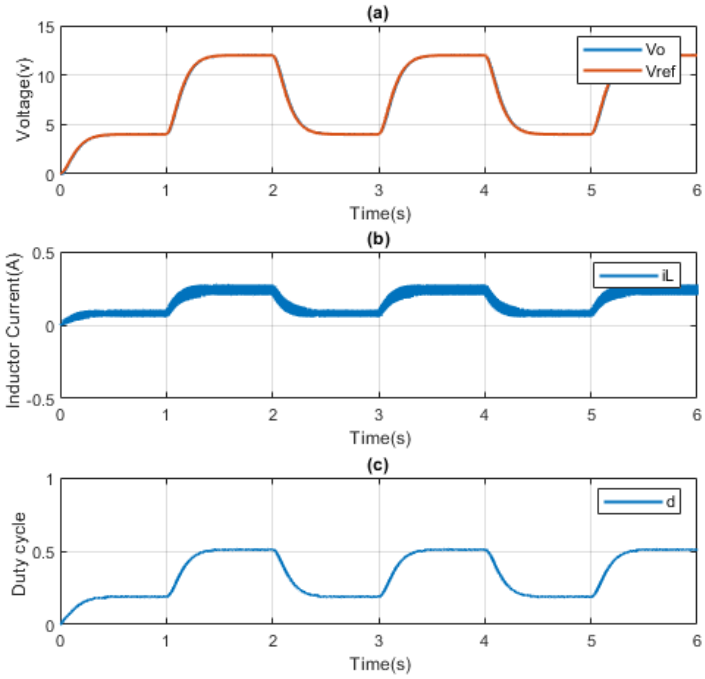


Figure 3.6: system response of Error-based ADRC for Buck-converter in (case 1)

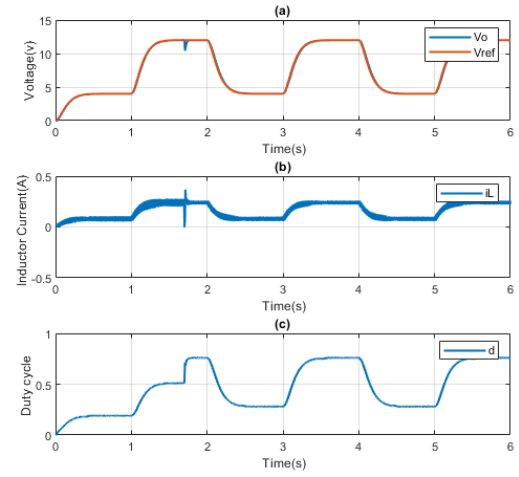
Result interpretation:

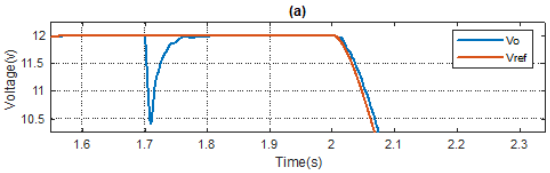
Figure 3.6 illustrates the performance of the Boost converter controlled using a single-loop, error-based Linear Active Disturbance Rejection Controller (LADRC), with a time-varying reference signal defined as:

$$v_{\text{ref}}(t) = 8 + 4 \cdot \text{square}(2\pi \cdot 0.5 \cdot t)$$

(a) The output voltage v_o effectively tracks the time-varying reference V_ref, With a quick response time and very little steady-state error. Excellent tracking performance is displayed by the controller, which manages the square-wave transitions smoothly and without overshoot or instability.
(b) The inductor current i_L remains stable and bounded throughout the simulation. It adjusts as needed to support the varying output voltage levels, without introducing oscillations or control saturation.
(c) The duty cycle d evolves continuously and smoothly, adapting in real-time to the reference changes. The absence of sharp discontinuities or chattering confirms the control stability and smooth operation of the LADRC.
These results indicate the stability of the LADRC controller in the presence of large and sudden reference changes. The built-in ESO can takewise estimate the uncertainties of systems in real time, the stability of system voltage is enhanced, and the control effect is not affected by accurate system model.

Case 2:

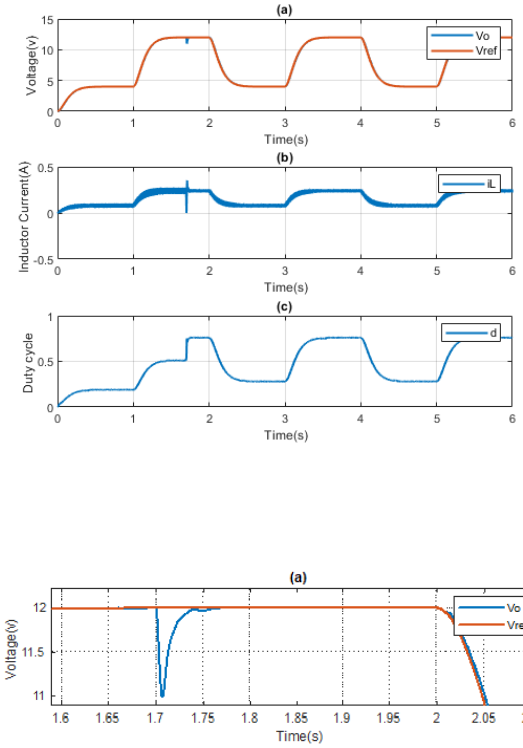




A cross-sectional image of the output voltage from case 2 to illustrate the duration of the compensation.

Figure 3.7: system response of Error-based ADRC for Buck-converter in (case 2) with $S^{ESO} = 5 \cdot S^{CL}$.

The observer poles were increased to accelerate the disturbance estimation and enhance the system's reaction. This helps to reduce the effect of the disturbance and improves the transient response. that's shown in Figure 3.8



A cross-sectional image of the output voltage from case 2 to illustrate the duration of the compensation.

Figure 3.8: system response of Error-based ADRC for Buck-converter in (case 2) with $S^{ESO} = 10 \cdot S^{CL}$.

Result interpretation:

In this case, the buck converter is controlled using an Error-based ADRC strategy,and a step disturbance is applied by decreasing the input voltage from $24v$ to $16v$ at $t = 1.7s$. the original observer pole placement at $S^{ESO} = 5 \cdot S^{CL} = -1500$,a small overshoot is observed in both the output voltage and the inductor current, lasting approximately $0.1s$ .also the duty cycle exhibits a minor transient deviation before stabilizing.
To analyze the influence of the ESO dynamics on disturbance rejection, the observer poles were increased to $S^{ESO} = 10 \cdot S^{CL} = -3000$, effectively doubling the observer Bandwidth. As a result, the overshoot in both voltage and the current significantly decreased in amplitude and duration, settling within $0.05s$.so about the duty cycle didn't change so much.
This behavior shows that the faster ESO observer (ESO pole placement) helps for accurate and faster estimation of disturbances and indicate that the controller would responses more accurately and earlier. As a result, the system has lower overshoot and better transient resoponse with no noise or instability become introduce. These results verify the vital importance of the ESO bandwidth adjustment to the robustness and speed of response of the ADRC.

Case 3:

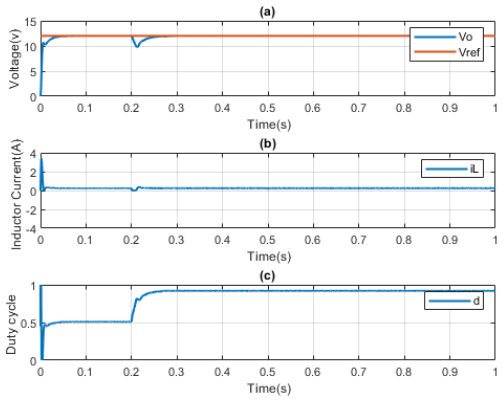


Figure 3.9: system response of Error-based ADRC for Buck-converter in (case 3) with $S^{ESO} = 5 \cdot S^{CL}$.

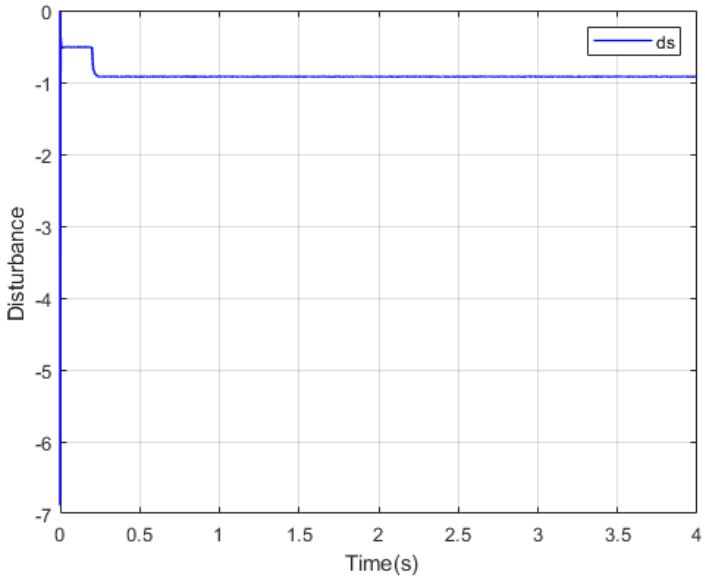


Figure 3.10: Normalized estimated disturbance

A step disturbance introduces a sudden change in the system 3.10, which remains constant at $t = 0.2$s after that drops quickly and fixed . that's mean This makes it easier for the ADRC observer to estimate and reject the disturbance correctly. its application. However, if the disturbance signal varies over time (e.g., sinusoidal or time-dependent load), the observer must continuously adapt to track its evolution..
When a step disturbance is applied (like a sudden input voltage drop), it changes instantly and then stays fixed. Since the disturbance no longer changes after that moment, it becomes constant over time. This makes it easier for the ADRC observer to estimate and reject the disturbance correctly.

Result interpretation

Figure 3.9. In this test, the reference voltage was set to 12 V, while a sudden input voltage drop was applied, changing the input from 24 V to 13 V at around $t = 0.2$ s.

In subplot (a), the output voltage briefly dips below the reference as the disturbance occurs. However, the controller quickly compensates and restores the voltage to its desired value without overshoot. This short transient is expected and highlights the momentary delay in the disturbance estimation, but the overall response remains fast and well-damped.

Subplot (b) shows the inductor current increasing immediately after the input voltage drops. This is consistent with the power balance, as the converter must draw more current to maintain the same output voltage when the input is reduced. After the initial spike, the current settles smoothly to a new steady-state level.

In subplot (c), the duty cycle increases sharply following the disturbance, reaching a higher value that allows the converter to maintain output regulation despite the lower input. Once the new operating point is reached, the duty stabilizes, and the system returns to steady-state behavior.

These results confirm that the error-based ADRC controller effectively manages sudden changes in input voltage. The fast recovery of the output voltage and stable current and duty responses demonstrate the controller's strong disturbance rejection and robustness in real-time conditions.

Case 4:

This simulation evaluates the robustness of the error-based ADRC in controlling a Buck converter under multiple simultaneous disturbances. Specifically, three events were introduced:

- A step decrease in input voltage from 24 V to 16 V at approximately $t = 1.1$ s.
- A step decrease in load resistance from 50 Ω to 25 Ω at approximately $t = 1.4$ s.
- A step change in the reference voltage from 10 V to 12 V at startup.

These variations test the controller's ability to ensure stability, accurate tracking, and effective disturbance rejection.

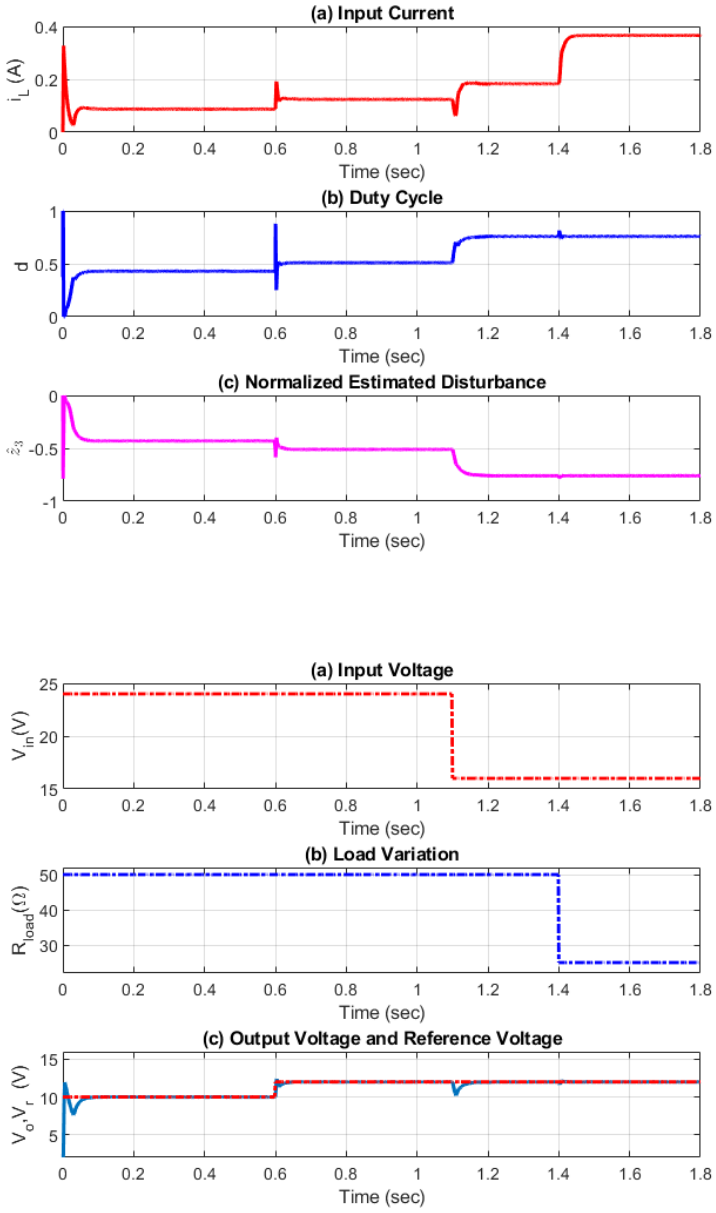


Figure 3.11: System response of Error-based ADRC for Buck-converter in (case 4).

- (a) The inductor current i_L reacts accordingly, increasing after the load drop due to higher power demand.
- (b) The duty cycle dynamically adjusts—first rising to compensate for the input voltage drop, then stabilizing after load variation.
- (c) The estimated disturbance $\hat{z}_3$ captures the effect of all variations and adapts in real time, validating the performance of the ESO in detecting and compensating for total disturbances.

The signals estimaed by the observer $\hat{z}_1$ and $\hat{z}_2$ were plotted in MATLAB in order

to illustrate the tracking error between the output voltage and the reference (z_1). This visualization helps evaluate the effectiveness of the ADRC in disturbance rejection and system stabilization.

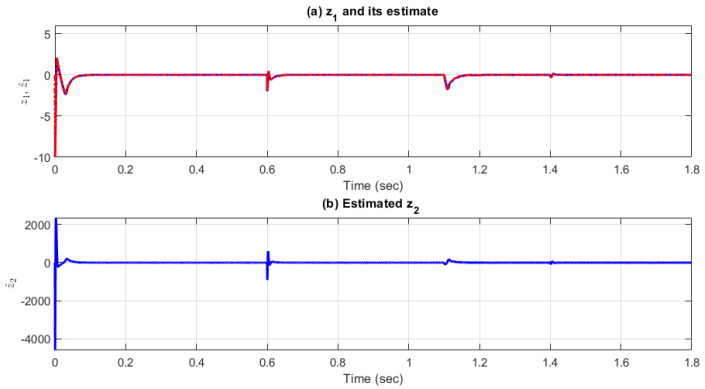


Figure 3.12: z_1 and Observer signals $\hat{z}_1$ and $\hat{z}_2$ in error-based ADRC control for Buck-converter.

MATLAB/SIMULINK

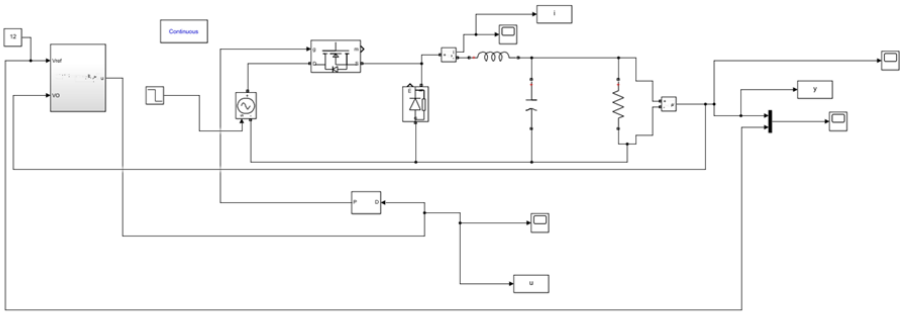


Figure 3.13: Screenshot MATLAB/SIMULINK circuit of Buck-converter by Error-based ADRC.

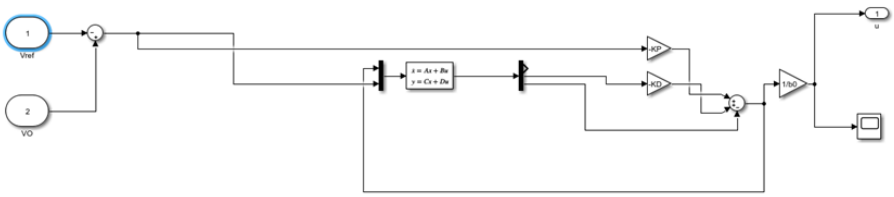


Figure 3.14: Screenshot MATLAB/SIMULINK Blocks of Error-based ADRC for Buck-converter.

3.2.5 Comparison with PI control

Analysis of Output Voltage Response (ADRC vs. PI)

The plots of Fig 3.15 illustrate how both controllers handle a sudden disturbance applied (input voltage(24V to 13V))at $t = 1.5s$ with reference 12V ,$R = 50\Omega$. The output voltage under ADRC control (subplot a) exhibits a very fast and minimal deviation, followed by a quick recovery to the reference level. The transient dip is small and short-lived, showing the real-time disturbance estimation and rejection capabilities of the ADRC's Extended State Observer (ESO).
In contrast,the proportional and integral gains ($K_p = 0$ and $K_i = 0.23218$) were selected using Simulink's built-in PID Tuner to ensure appropriate closed-loop behavior with settling time $T_{settle} = 0.7s$. the PI controller response (subplot b) reveals a larger and slower deviation when the disturbance is introduced. The output drops significantly and requires more time to return to the desired value. This reflects the PI controller's lack of internal disturbance estimation, making it rely solely on feedback error, which leads to slower correction and more sensitivity to unexpected system changes.

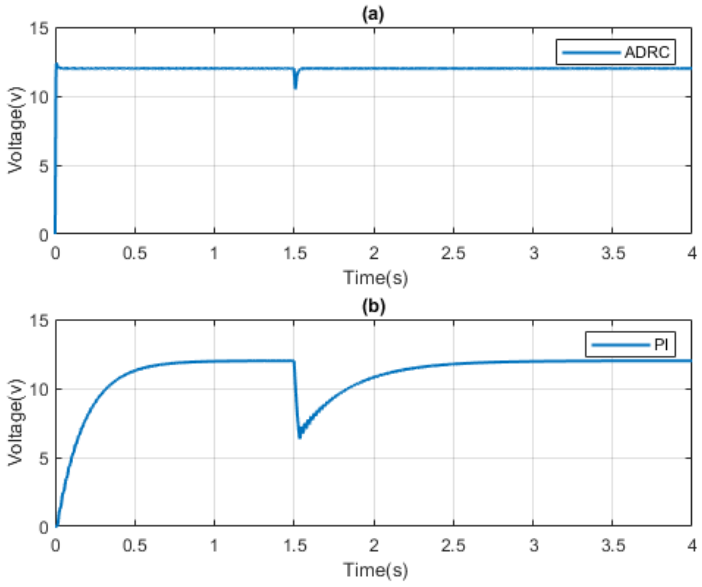


Figure 3.15: Output voltage response (ADRC vs. PI)

3.3 ADRC-based Control of Boost converter

In this section, an Active Disturbance Rejection Control (ADRC) strategy is applied to regulate the output voltage of a DC/DC Boost converter,the simulation of the system under study in MATLAB/SIMULINK and analysis of the simulation findings achieved. Due to the converter's nonlinear and non-minimum phase characteristics, a cascade control structure is adopted. The inner loop is designed to control the inductor current, while the outer loop regulates the output voltage. Each loop is equipped with a dedicated Extended State Observer (ESO) to estimate and reject internal and external disturbances in real time. This cascade ADRC approach improves the dynamic

response and enhances the robustness of the system under load and input voltage variations.The Boost converter is a nonlinear switching converter used to step up a DC voltage. Its behavior can be represented using an averaged model over one switching period. Assuming continuous conduction mode (CCM), the state-space averaged equations (3.1) of the Boost converter are given by:

$$\begin{cases} \frac{di_L}{dt} = \frac{V_{\text{in}}}{L} - \frac{(1-d)}{L} V_O \\ \frac{dV_O}{dt} = \frac{1-d}{C} i_L - \frac{V_O}{RC} \end{cases} \tag{3.1}$$

Where:

- i_L is the inductor current (A),
- V_O is the output voltage across the capacitor (V),
- V_{in} is the input voltage source (V),
- d is the duty cycle, a control input signal in the range $[0, 1]$

This averaged model is used for controller design and analysis by replacing the switching behavior with continuous-time equations. The duty cycle d determines the amount of energy transferred from the inductor to the output during each switching cycle. the Boost-converter is modeled using the following component values:

Table 3.4: Physical Parameters of the Boost-Converter

Symbol	**Value**	**Unit**	**Description**
R	50	Ω	Load resistance
L	1	mH	Inductor
C	920	μF	Output capacitor
f_{sw}	10	KHz	Switching Frequency
V_{in}	12	V	Input voltage
V_{ref}	24	V	Output voltage
$d_{nominal}$	0.5		d pour V_{ref}=24v et V_{in}=12v

These values are adopted from a reference study presented in [12].

Controller design method

3.3.1 Cascade Control for Boost-converter

This study develops an inner-loop current controller and an outer-loop voltage controller based on Active Disturbance Rejection Control (ADRC) for the average model of the DC/DC Boost converter. The structure features two-channel control, feedback compensation, and disturbance rejection. The Extended State Observer (ESO) is employed to estimate disturbances, which are then suppressed via real-time compensation. The capacitive voltage and inductor current signals serve as feedback to the outer and inner loops, respectively..the modeling methodology presented in this section is adapted from the work of [12].

1. **Design of voltage controller:**

   The output voltage dynamics are modeled as:

$$\frac{dV_O}{dt} = \frac{1-d}{C} i_L - \frac{V_O}{CR} + d_s(t) \tag{3.2}$$

   that: $d_s(t)$ is a disturbance.
   Let $V_O = y_1$, and $u_1 = i_L$, then:

$$\dot{y}_1 = \frac{1-d}{C} u_1 - \frac{V_O}{CR} + d(t) = b_1 u_1 + f_1(y_1, u_1) \tag{3.3}$$

   Where:

$$b_1 = \frac{1-d}{C}, \quad f_1 = -\frac{V_O}{CR} + d_s(t)$$

   Let $x_1 = y_1$, $x_2 = f_1$, then:

$$\begin{cases} \dot{x} = A_1 x + B_1 u_1 + E_1 \dot{f}_1 \\ y_1 = C_1 x \end{cases} \tag{3.4}$$

$$A_1 = \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix}, \quad B_1 = \begin{bmatrix} b_1 \\ 0 \end{bmatrix}, \quad E_1 = \begin{bmatrix} 0 \\ 1 \end{bmatrix}, \quad C_1 = \begin{bmatrix} 1 & 0 \end{bmatrix}$$

   Second-order ESO

$$\begin{cases} \dot{\hat{x}} = A_1 \hat{x} + B_1 u_1 + L_{01}(y_1 - \hat{y}_1) \\ \hat{y}_1 = C_1 \hat{x} \end{cases} \tag{3.5}$$

   Where:

$$L_{01} = \begin{bmatrix} \beta_{11} \\ \beta_{12} \end{bmatrix}$$

   Control Law

   Using proportional control:

$$u = k_1(r_1 - \hat{x}_1) \tag{3.6}$$

   The final control law is created as follows in order to automatically compensate for the entire disturbance:

$$u_1 = \frac{k_1(r_1 - \hat{x}_1) - \hat{x}_2}{b_1} \tag{3.7}$$

   Substituting Equation (3.12) into Equation (3.8):

$$\dot{y}_1 = u - \hat{x}_2 + f_1 \approx u$$

ESO Tuning Parameters

To meet the desired voltage loop settling time $T_{\text{settle,voltage}}$:

$$K_1 = \frac{4}{T_{\text{settle,voltage}}}, s_1^{CL} = -k_1, \quad s^{ESO1} = (3 \dots 10) \cdot s_1^{CL}$$
$$\beta_{11} = -2s^{ESO1}, \quad \beta_{12} = (s^{ESO1})^2$$

2. **Design of current controller:** The Boost converter's average current dynamics are expressed as:
$$\frac{di_L}{dt} = \frac{V_{\text{in}}}{L} - \frac{(1-d)}{L} V_O \tag{3.8}$$
Let $i_L = y_2$, $d = u_2$, then:
$$\dot{y}_2 = -\frac{1}{L} V_O u_2 + \left(\frac{V_{\text{in}}}{L} - \frac{1}{L} V_O \right) = b_2 u_2 + f_2(y_2, u_2) \tag{3.9}$$
Where:
$$b_2 = \frac{V_O}{L}, \quad f_2 = \frac{V_{\text{in}}}{L} - \frac{1}{L} V_O$$
Let $x_1 = y_2$, $x_2 = f_2$, then the state-space model becomes:
$$\begin{cases} \dot{x} = A_2 x + B_2 u_2 + E_2 \dot{f}_2 \\ y_2 = C_2 x \end{cases} \tag{3.10}$$
With matrices:
$$A_2 = \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix}, \quad B_2 = \begin{bmatrix} b_2 \\ 0 \end{bmatrix}, \quad E_2 = \begin{bmatrix} 0 \\ 1 \end{bmatrix}, \quad C_2 = \begin{bmatrix} 1 & 0 \end{bmatrix}$$

Second-order ESO

$$\begin{cases} \dot{\hat{x}} = A_2 \hat{x} + B_2 u_2 + L_{02}(y_2 - \hat{y}_2) \\ \hat{y}_2 = C_2 \hat{x} \end{cases} \tag{3.11}$$
Where:
$$L_{02} = \begin{bmatrix} \beta_{21} \\ \beta_{22} \end{bmatrix}$$

Control Law

As the system has a relative degree of one, the control law is:

$$u' = k_2(r_2 - \hat{x}_1) \tag{3.12}$$

Here, $\hat{x}_2 = \hat{f}_2$ is estimated by the LESO. To automatically compensate the total disturbance, the final control law is:

$$u_2 = \frac{u' - \hat{x}_2}{b_2} = \frac{k_2(r_2 - \hat{x}_1) - \hat{x}_2}{b_2} \tag{3.13}$$

Where r_1 is the reference input, and k_1 is the proportional gain.

We get from Equation (3.6) in Equation (3.2):

$$\dot{y}_2 = u' - \hat{x}_2 + f_2 \approx u'$$

If $\hat{y}_2(t) \approx y_2(t)$, then we obtain a first-order closed-loop behavior with a pole:

$$s_2^{CL} = -K_2$$

ESO Tuning Parameters

To achieve desired settling time $T_{\text{settle,current}}$, use:

$$K_2 = \frac{4}{T_{\text{settle,current}}}, \quad s^{ESO2} = (3 \dots 10) \cdot s_2^{CL}$$
$$\beta_{21} = -2s^{ESO2}, \quad \beta_{22} = (s^{ESO2})^2$$

3.3.2 Simulation Results of cascade control for Boost-converter

In the cascade ADRC controller, two independent loops are implemented:
An outer voltage loop, responsible for regulating the output voltage.
An inner current loop, responsible for tracking the reference current generated by the outer loop.
The ADRC parameters utilized in both loops are maintained consistent throughout all simulation situations for uniformity and an equitable performance comparison. Each loop's design is based on a set settling time target (Tsettle), which establishes the dynamics of the observer and controller.

- for the outer loop and the inner loop, the settling time is the same:

$$T_{\text{settle,voltage,current}} = 0.02 \text{ s}$$

The poles of (ESO) for the outer loop are placed at:

$$s^{ESO2} = (3) \cdot s_2^{CL} = -600$$

$$\beta_{11} = -2s^{ESO2} = 1200, \quad \beta_{12} = (s^{ESO2})^2 = 360000$$

- For the current loop, The ESO poles are :

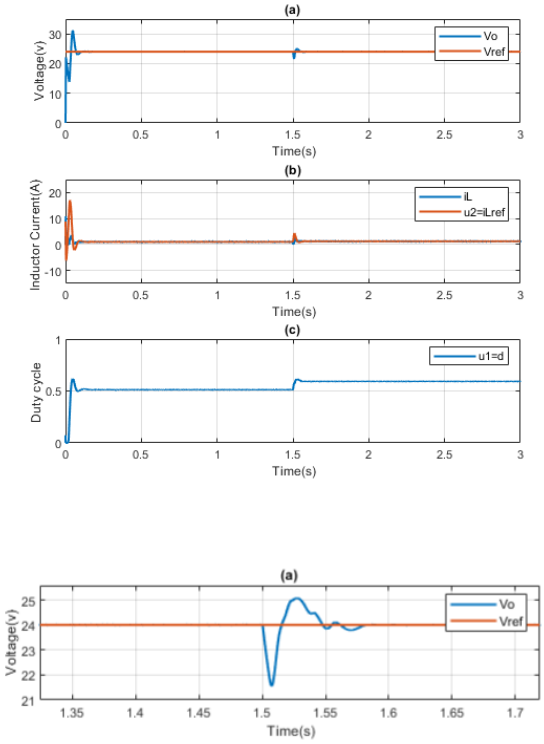
$$s^{ESO1} = (3) \cdot s_1^{CL} = -1000$$

$$\beta_{21} = -2s^{ESO2} = 2000, \quad \beta_{22} = (s^{ESO2})^2 = 1000000$$

The controller gains are computed accordingly $b_1 = \frac{1-d}{C} = 543.4783$, $b_2 = V_O/L = 24000$ and remain constant throughout the different test cases to provide a fair performance comparison under:

Case 1: Input voltage variation This simulation demonstrates the performance of a Boost converter controlled using a cascade Active Disturbance Rejection Control (ADRC) approach. The system is subjected to a disturbance in the form of a step change in the input voltage from $12v$ to $10v$ around $t = 1.5$ s, while the output voltage reference remains constant. The ADRC controller's objective is to maintain the output voltage regulation and ensure fast recovery in the presence of such disturbances.fig 3.16

- **(a)** shows the output voltage V_o and its reference V_{ref}.
- **(b)** displays the inductor current i_L and the inner-loop current reference u_2.
- **(c)** presents the duty cycle $u_1 = d$, which is the control input applied to the converter switch.



(a) A cross-sectional image of the output voltage from case 1 of Boost-converter to illustrate the duration of compensation

Figure 3.16: System response under cascade control ADRC for Boost-converter in case 1.

Result interpretation

- **Output Voltage V_o (subplot a):** The voltage initially stabilizes quickly around the reference. At $t \approx 1.5$ s, the system experiences a clear disturbance due to a step change in the input voltage. The ADRC controller responds rapidly, and the output voltage quickly returns to the reference, confirming strong disturbance rejection and dynamic robustness.

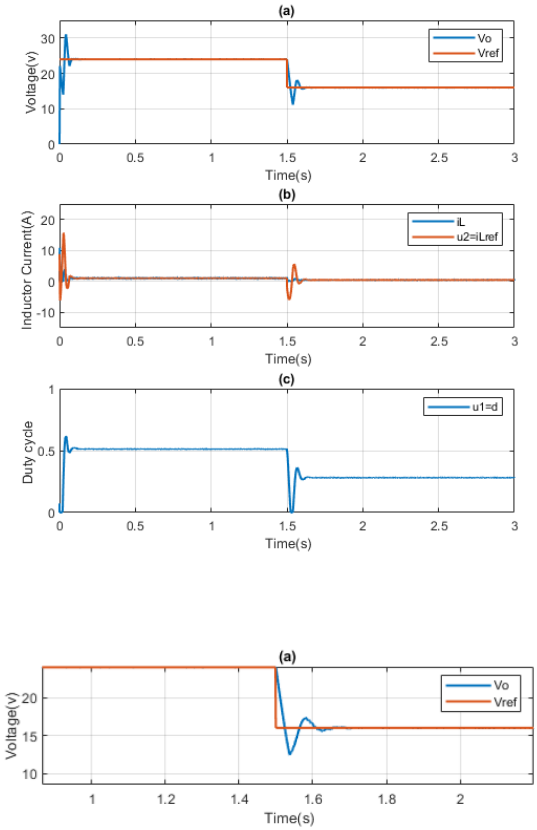
- **Inductor Current i_L (subplot b):** The current tracks the reference with a transient during the input change, but it recovers quickly. The shape and alignment with u_2 demonstrate effective current control under input perturbation.

- **Duty Cycle d (subplot c):** The duty cycle adjusts dynamically in response to the input voltage drop — increasing to compensate and maintain the output voltage. After the disturbance, the signal stabilizes, showing proper actuator behavior and responsiveness of the ADRC control law.

Case 2: Reference variation

To test the controller's performance under reference changes, a step variation is applied to the output voltage reference from $24v$ to $16v$ at time $t = 1.5\,\text{s}$. This allows

evaluation of the controller's dynamic response and disturbance rejection capability during sudden setpoint changes.



(a) A cross-sectional image of the output voltage from case 2 of Boost-converter to illustrate the duration of compensation

Figure 3.17: System response under cascade control ADRC for Boost-converter in case 2.

Result interpretation

- The output voltage successfully follows the reference value with good dynamic response and minimal steady-state error.
- The inductor current tracks its reference accurately, even reference changes.
- The duty cycle control input varies smoothly, adjusting effectively to maintain the desired output.

At the reference change instant, small transients appear, but the system quickly stabilizes, confirming the good performance of the cascade ADRC controller in terms of fast response, robustness, and disturbance rejection.

MATLAB/SIMULINK

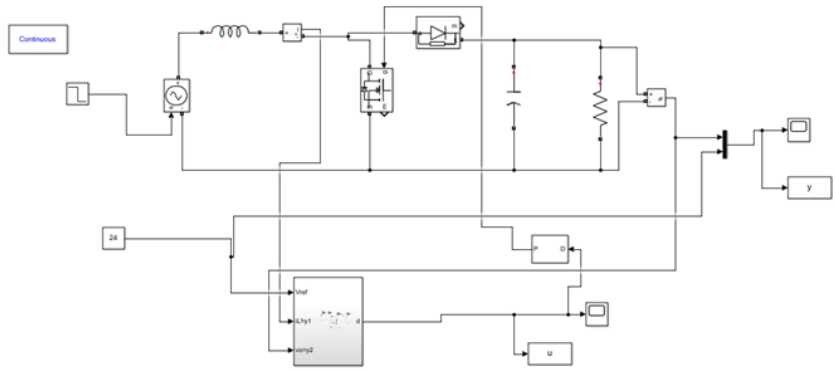


Figure 3.18: Screenshoot MATLAB/SIMULINK circuit of Boost-converter by Cascade design ADRC.

Matlab/Simulink Blocks of Boost for Cascade control design is the same forma with fig 3.5

3.3.3 Error-Based ADRC for Boost-converter

In this approach, we design an Active Disturbance Rejection Controller (ADRC) for a Boost converter by error-based strategies. The control focuses on regulating the output voltage while effectively rejecting disturbances and accounting for the nonlinear characteristics of the Boost topology.

Averaged Model of Boost Converter

We consider the state variables:

$$x_1 = i_L, \quad x_2 = V_o$$

The averaged state-space equations are:

$$\begin{cases} \dot{x}_1 = \frac{-(1-d)}{L} x_2 + \frac{V_{\text{in}}}{L} \\ \dot{x}_2 = \frac{(1-d)}{C} x_1 - \frac{1}{RC} x_2 \end{cases} \tag{3.14}$$

as we saw in the part of Cascade control for Boost-converter that the gain input for each equation is :

- for the current equation : $b_1 = \frac{V_O}{L}$
- for the voltage equation: $b_2 = \frac{1-d}{C}$

Error-Based ADRC Reformulation

Let us define the error:

$$z_1 = V_o - V_{ref} = x_2 - V_{\text{ref}}$$

Taking the derivative:

$$\dot{z}_1 = \dot{x}_2 = \frac{(1-d)}{C}x_1 - \frac{1}{RC}x_2 = z_2 \tag{3.15}$$

Now taking the second derivative:

$$\begin{aligned}\ddot{z}_1 = \dot{z}_2 &= \frac{d}{dt}\left(\frac{(1-d)}{C}x_1 - \frac{1}{RC}x_2\right) \\ &= \frac{(1-d)}{C}\dot{x}_1 - \frac{1}{RC}\dot{x}_2\end{aligned}$$

Substitute $\dot{x}_1$ and $\dot{x}_2$:

$$\begin{aligned}\dot{z}_2 &= \frac{(1-d)}{C}\left(\frac{-(1-d)}{L}x_2 + \frac{V_{\text{in}}}{L}\right) - \frac{1}{RC}\left(\frac{(1-d)}{C}x_1 - \frac{1}{RC}x_2\right) \\ &= \frac{(1-d)}{C}\cdot\frac{1}{L}x_2\cdot d - \frac{(1-d)}{C}\cdot\frac{1}{L}x_2 + \frac{(1-d)}{C}\cdot\frac{v_{in}}{L} - \frac{(1)}{RC}\cdot\dot{x}_2\end{aligned}$$

Let the total disturbance be:

$$f = \dot{z}_2 - b_0 d$$

Let the control input be:

$$u = d$$

Hence, the system becomes the following:

$$\dot{z}_2 = b_0 u + f$$

Extended State Observer (ESO)

We define the extended states:

$$\begin{aligned}\dot{z}_1 &= z_2 \\ \dot{z}_2 &= b_0 u + \hat{f} \\ \dot{z}_3 &= \dot{f}\end{aligned}$$

The ESO dynamics are as follows:

$$\begin{cases}\dot{\hat{z}}_1 = \hat{z}_2 + L_1(z_1 - \hat{z}_1) \\ \dot{\hat{z}}_2 = b_0 u + L_2(z_1 - \hat{z}_1) \\ \dot{\hat{z}}_3 = L_3(z_1 - \hat{z}_1)\end{cases} \tag{3.16}$$

Matrix form:

$$\begin{bmatrix}\dot{\hat{z}}_1 \\ \dot{\hat{z}}_2 \\ \dot{\hat{z}}_3\end{bmatrix} = \underbrace{\begin{bmatrix}-L_1 & 1 & 0 \\ -L_2 & 0 & 1 \\ -L_3 & 0 & 0\end{bmatrix}}_{A-LC}\begin{bmatrix}\hat{z}_1 \\ \hat{z}_2 \\ \hat{z}_3\end{bmatrix} + \begin{bmatrix}0 \\ b_0 \\ 0\end{bmatrix} u + \begin{bmatrix}L_1 \\ L_2 \\ L_3\end{bmatrix} y$$

Control Law

To achieve a fast and stable response, the control law is designed as:

$$u(t) = \frac{u_0 - \hat{f}(t)}{b_0}, \quad \text{with} \quad u_0 = -K_P z_1 - K_D \hat{z}_2 - \hat{z}_3$$

Where:

- r is the voltage reference
- b_0 is an estimated control gain, e.g., $b_0 = \frac{(1-d)V_o}{LC}$
- as we see that $b_0 = b_1 \cdot b_2$ where b_1 and b_2 from the cascade control for boost converter.

Tuning Controller Gains

To achieve a critically damped second-order closed-loop behavior with 2% settling time T_{settle}, use:

$$s_{1,2}^{CL} = s^{CL} \approx -\frac{6}{T_{\text{settle}}}$$

$$K_P = (s^{CL})^2, \quad K_D = -2s^{CL}$$

ESO Gain Design

Choose the observer poles as:

$$s_{1,2,3}^{ESO} = s^{ESO} \in [3, 10] \cdot s^{CL}$$

The characteristic polynomial of $(A - LC)$ is:

$$\det(sI-(A-LC)) = s^3+L_1s^2+L_2s+L_3 = (s-s^{ESO})^3 = s^3-3s^{ESO}s^2+3(s^{ESO})^2s-(s^{ESO})^3$$

Matching coefficients, the ESO gains are:

$$L_1 = -3s^{ESO}, \quad L_2 = 3(s^{ESO})^2, \quad L_3 = -(s^{ESO})^3$$

This completes the design of ADRC strategy that leverages the error-based structure for fast implementation and to reject total disturbances dynamically in the Boost converter.

3.3.4 Simulation Results of Error-based ADRC for Boost-converter

This section presents the simulation results of applying the error-based Active Disturbance Rejection Control (ADRC) to a Boost converter. The objective is to regulate the output voltage while rejecting disturbances such as input voltage variations and reference changes. The controller performance is evaluated in terms of tracking accuracy, disturbance rejection, and dynamic response. 3.5

Table 3.5: Computed Error-based ADRC parameters for Boost-converter based on $T_{\text{settle}} = 0.02$ s

Parameter	**Expression**	**Value**
s^{cl}	$-6/T_{\text{settle}}$	-300
K_P	s_{cl}^2	90 000
K_D	$-2 \cdot s_{\text{cl}}$	600
s^{ESO}	$5 \cdot s_{\text{cl}}$	-900
L_1	$-3 \cdot s_{\text{ESO}}$	2700
L_2	$3 \cdot s_{\text{ESO}}^2$	2430000
L_3	$-s_{\text{ESO}}^3$	729×10^6
b_0	$(1-d) \cdot V_{ref}/(C \cdot L)$	$1.3043e+07$

The simulation involves a Boost converter that is regulated by an error-based ADRC, is subjected to two step changes.fig 3.20:

- A step change in the **input voltage** from 12 V to 8 V at $t = 1.1$ s, simulating a source disturbance.
- A step decrease in the **reference output voltage** V_{ref} from 20 V to 24 V at $t = 0.6$ s. item A step change in the **resistance** from 50 Ω to 25 Ω at $t = 1.4$ s,

Result Interpretation

These changes test the ADRC controller's ability to maintain output voltage regulation and reject disturbances in real-time operation.as we see in fig 3.20

- **Output Voltage V_o (subplot a):** The output voltage follows the reference accurately during the initial steady-state. At $t \approx 1$ s, the input voltage change causes a brief ripple, which is quickly corrected. After the reference voltage increase at $t = 0.6$ s, V_o tracks the new reference rapidly with minimal undershoot, highlighting the robustness and responsiveness of the ADRC controller.
- **Inductor Current i_L (subplot b):** The current slightly increases in response to the increased reference voltage variation and then decreases smoothly as the input voltage drops, also the current doubles when the load resistance changes half. The system maintains stability throughout both events, with no oscillations or divergence observed.
- **Duty Cycle d (subplot c):** The duty cycle increases at $t \approx 0.6$ s appropriately in response to the higher output voltage reference, as expected in Boost converter behavior. At $t = 1.1$ s,then it decreases to compensate the input voltage drops,Finally the duty decreases when the load drops. These dynamics confirm that the controller actively adjusts the control input to preserve system performance.

The signals z_1 and $\hat{z_1}$ and $\hat{z}_2$ were plotted in MATLAB in order to illustrate the tracking error between the output voltage and the reference (z_1). When a step disturbance is applied (like a sudden input voltage drop), it changes instantly and then stays

fixed.Since the disturbance no longer changes after that moment, it becomes constant over time. This makes it easier for the ADRC observer to estimate and reject the disturbance correctly.in fig 3.19

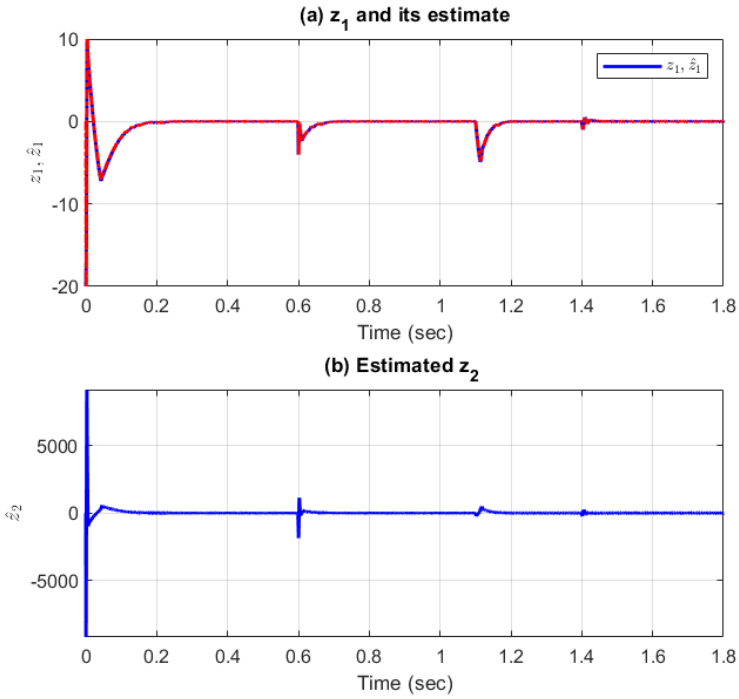
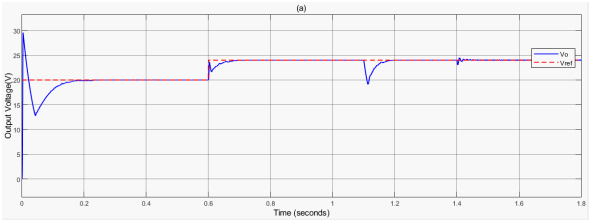
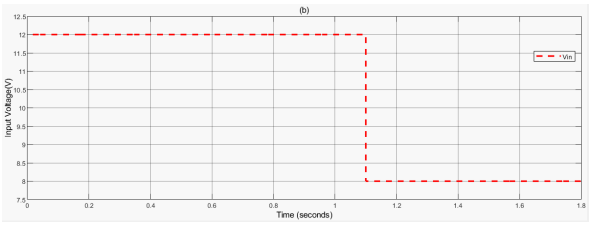


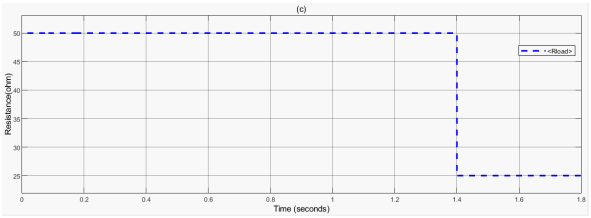
Figure 3.19: z_1 and Observer signals $\hat{z}_1$ and $\hat{z}_2$ in Error-based ADRC for Boost-converter.



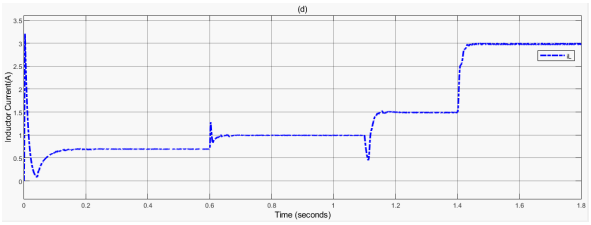
(a) Output voltage response



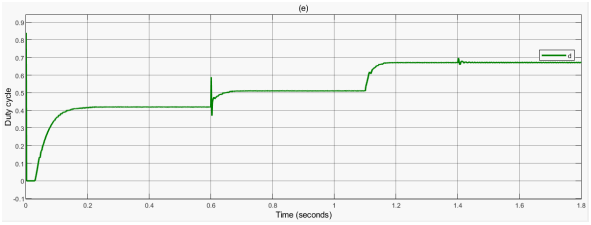
(b) Input voltage variation



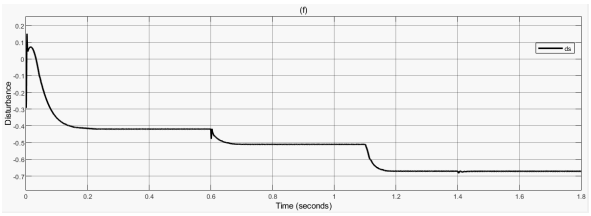
(c) Load variation



(d) Output current response



(e) Duty ratio



(f) Normalized Estimated disturbance

Figure 3.20: system response under Error-based ADRC for Boost-converter

MATLAB/SIMULINK

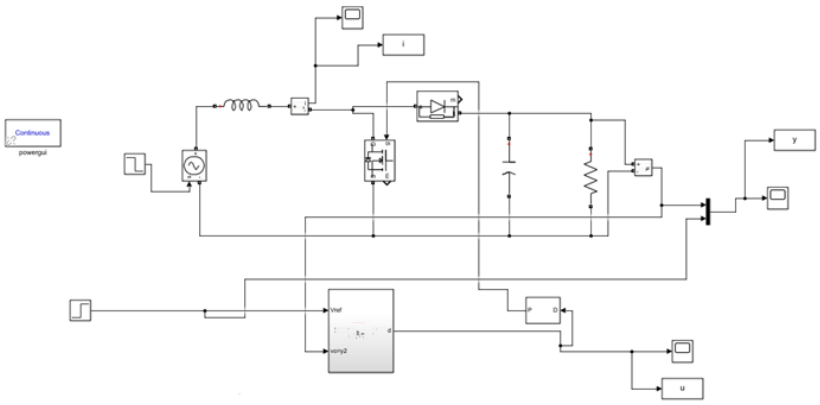


Figure 3.21: Screenshot MATLAB/SIMULINK circuit of Error-based ADRC for Boost-converter.

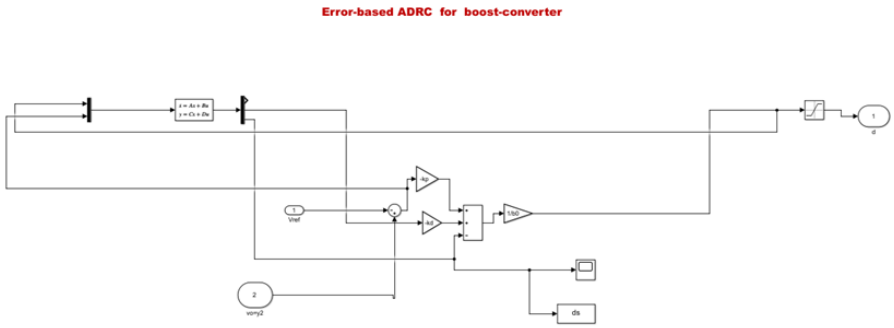


Figure 3.22: Screenshot MATLAB/SIMULINK Blocks of Error-based ADRC for Boost-converter.

3.4 Conclusion

This work has presented the control of Buck and Boost converters using Active Disturbance Rejection Control (ADRC) through both cascade and error-based structures. For the Buck converter, the cascade ADRC method effectively regulated the output voltage by employing an inner current loop and an outer voltage loop. This structure ensured fast dynamic response and strong robustness to disturbances, particularly when variations in the input voltage or load occurred. Similarly, the error-based ADRC applied to the Buck converter demonstrated smoother duty cycle behavior and fast reference tracking, while slightly slower in disturbance estimation due to its single-loop structure.

For the Boost converter, both control strategies were also implemented and analyzed. The cascade ADRC showed excellent performance in rejecting disturbances and handling changes in reference and input voltage. The dual-loop structure allowed

for improved current shaping and voltage regulation under non-minimum phase conditions. The error-based ADRC, on the other hand, offered a simpler architecture and demonstrated fast compensation of disturbances with a smooth and stable control signal, although the inductor current was slightly rougher during transients.

In all tested scenarios, ADRC has proven to be a highly robust control method, capable of estimating and rejecting internal and external disturbances in real-time. The use of Extended State Observers (ESOs) enabled the reconstruction of unknown dynamics, allowing the controllers to maintain output stability and performance despite system uncertainties, abrupt changes in input voltage, or load variations. Overall, ADRC provided better disturbance rejection and adaptability compared to traditional controllers, confirming its suitability for nonlinear power converter applications.

Chapter 4

Experimental validation for Buck-converter ADRC control

4.1 Introduction

After the simulating results that confirms the control approaches, this chapter demonstrates the experimental realization of ADRC for Buck converter.The experimental equipment consists in a dSPACE1104 control, which is in communication through Control Desk with a host PC,It is comprised of a programmable power supply, a driver circuit to boost control signals and a programmable power electronics box working in Buck. Voltage and current sensors transmit feedback signals to the controller for closed loop operation. The hardware and software used are explained, the control development process is described, and finally real-life disturbance and parameter variation are presented to confirm the robustness and performance of the ADRC strategy.

4.2 Experimental Description

The dSPACE DS1104 board was used as the real-time control platform to implement the ADRC controller, acquire sensor signals, and generate PWM signals to drive the Buck converter. to validate the performance of the designed Active Disturbance Rejection Controller (ADRC) for a Buck converter, a real-time experimental setup was implemented using the following components:

4.2.1 DSPACE DC1104

The control board A piece of hardware called the DS1104 guarantees quick and effective control while enhancing PC performance. Since DS1104 is reasonably priced and an ideal development system for both industry and academia, it provides :

- A powerPC processor for real-time control execution.
- An ADC/DAC interface for signal acquisition and generation.
- Integration with MATLAB/Simulink via Real-Time interface (RTI) blocks, allowing direct deployment of the control model.

the PC is connected to the DSPACE DS1104 via a PCI slot, and simulink models are compiled and downloaded to the board using DS1104 ControlDesk or RTI.

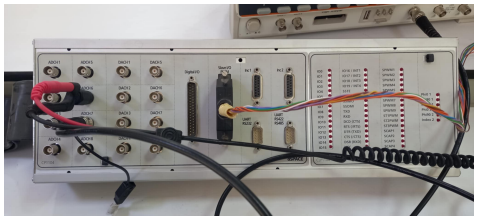


Figure 4.1: DSPACE DS1104

Composition of the card DS1104

Two processors (master and slave), interrupt controllers, memory, delays, and interfaces are all included in the DS1104 single-board system. [13] The DS1104's architecture is summarized in the following illustration:

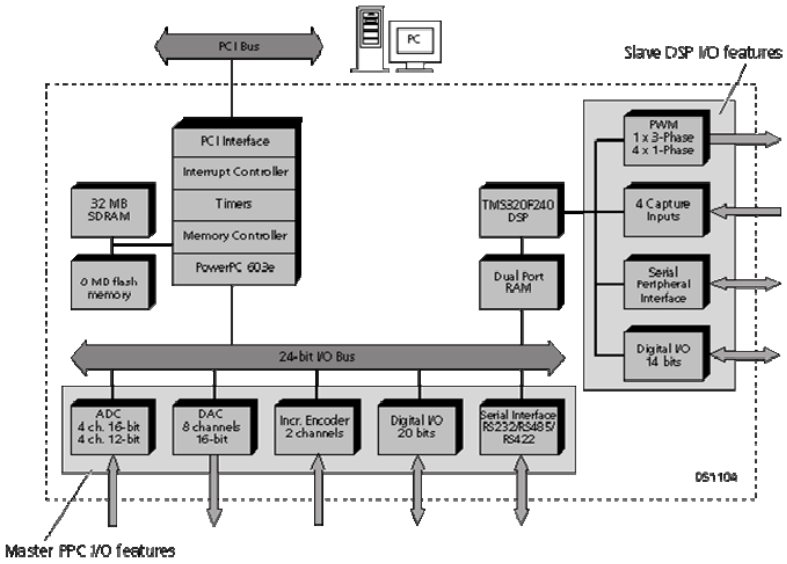


Figure 4.2: Architecture of the DSPACE DS1104 card

Table 4.1: Main technical features of DSPACE DS1104 used in this project

Processor	250 MHz PowerPC.
Analog Inputs	16-bit resolution.
PWM Outputs	1 channel (used for Buck control to generate the duty cycle).
Interface	Simulink Real-Time Workshop, ControlDesk.
ADC (Analog-to-Digital Converter)	For reading voltage and current from sensors.
DAC (optional)	For signal monitoring (e.g., ControlDesk plots).

4.2.2 IGBT Half-Bridge Module as a Buck Converter

The experimental configuration used a programmable power electronics module based on an IGBT half-bridge that fined the Buck converter topology. While this module has been designed for inverter or chopper use, it can be adapted without difficulty to work as a step-down DC/DC converter by simply selecting an appropriate passive network.

configuration

- The half-bridge contains two IGBT switches with anti-parallel diodes.
- In the Buck topology there is only IGBT switch to produce the PWM signal.
- The current is conducted during the turn-off state through a freewheeling diode (either the internal diode of the lower IGBT or an external diode).
- Input was the boost rail, output was the classic buck.
- The input voltage (24 V) was supplied by a DC source and the switching was driven by the PWM signal from the DS1104.

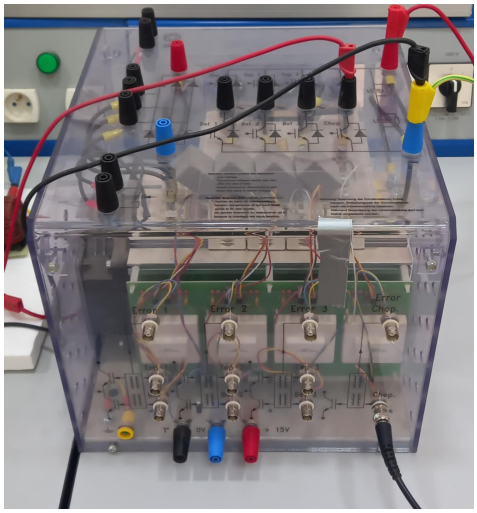


Figure 4.3: Hlaf bridge IGBT.

4.2.3 Driver Interface Board (Signal Conditioning and Amplification Module)

The dSPACE DS1104 digital outputs were interfaced with the power converter's gate-driver inputs via a specially designed driver board. This board has several uses.

- **Signal Amplification:** The DS1104 produces digital control signals (like PWM) that are amplified and conditioned to meet the gate driver stage of the power converter's voltage and current requirements.
- **Isolation and Protection:** The driver board isolates low-voltage control signals from high-power switching elements, reducing noise and protecting the dSPACE hardware.
- **Connectivity:** The board offers standard terminal blocks for flexible connecting to the converter stage and is connected to the DS1104 via a flat ribbon connection.

Table 4.2: Experimental Setup Specifications

Component	**Description**
Power Supply	24 V DC regulated input
Sensors	Voltage and current measurement, feedback to dSPACE
Oscilloscope	Used to observe the duty cycle signal in real time
RLC Parameters	Chosen based on ripple constraints to ensure stability and good performance

4.2.4 circuit parameters for buck converter

The passive component values (L and C) were selected external to connect them with the IGP based on standard ripple design rules to limit inductor current ripple to acceptable levels (e.g., 20–30%).

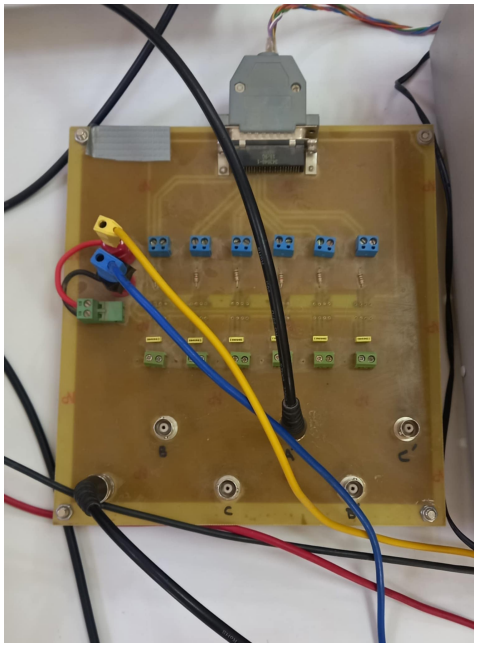


Figure 4.4: Drive Interface Board.

Inductor and Capacitor Selection [14]

In the Buck converter design, the inductor ripple current Δi_L is typically chosen as a fraction of the maximum load current:

$$\Delta i_L = 20\% \times I_{\text{max}} = 0.2 \times 1 \text{ A} = 0.2 \text{ A}$$

This choice represents a good trade-off between system size, cost, and output voltage ripple.

Inductance Calculation

The required inductance is calculated using the ripple current formula:

$$L = \frac{(V_{\text{in}} - V_{\text{out}}) \cdot D \cdot T_s}{\Delta i_L}$$

Where:

- $V_{\text{in}} = 24$ V is the input voltage
- $V_{\text{out}} = 12$ V is the desired output
- $D = \frac{V_{\text{out}}}{V_{\text{in}}} = 0.5$ is the duty cycle
- $T_s = \frac{1}{f_{\text{sw}}} = \frac{1}{20000} = 50$ μs

Thus:

$$L = \frac{V_{\text{OUT}} \times (V_{\text{IN}} - V_{\text{OUT}})}{\Delta I_L \times f_S \times V_{\text{IN}}} \tag{4.1}$$

we get:

$$L = \frac{12 \cdot (24 - 12)}{0.2 \cdot 20000 \cdot 24} = 1.5 \text{ mH}$$

In this work, we have chosen the value of the available inductance $L = 1.6$ mH, which is proportional to the calculated value.

Capacitance Calculation [14]

The output capacitor is sized based on acceptable voltage ripple ΔV_{out}:

$$C = \frac{\Delta i_L}{8 \cdot f_{\text{sw}} \cdot \Delta V_{\text{out}}}$$

Assuming $\Delta V_{\text{out}} = 1\% \times V_{\text{max}} = 0.01 \times 12 \text{ V} = 0.12 \text{ V}$, we get:

$$C = \frac{0.2}{8 \cdot 20000 \cdot 0.0015} = 104 \ \mu\text{F}$$

4.3 Hardware Experiment

4.3.1 Testbed description

The Buck converter was controlled by ADRC use 3.2.3,The experimental setup used for the study is seen in Fig 4.5. The control algorithm was implemented in MATLAB/Simulink platform, in which the system were modeled with error-based ADRC models. The model was run on a dSPACE DS1104 real-time controller hosted by a PC. The PWM duty cycle corresponding to the ADRC control output was generated by the DS1104 and passed to a driver circuit.
Current and voltage of the inductor were sensed, which were acquired as the feedback signals through the analog inputs of the dSPACE 1104 board. These were utilized for real-time control and were additionally displayed on the PC and recorded via ControlDesk. Although the duty cycle signal was also seen on a digital oscilloscope to verify the result, the entire system behavior (output voltage, inductor current and duty cycle) was recorded and plotted on ControlDesk.
The electrical parameters of the Buck converter used in the experimental setup were chosen according to standard design rules to ensure effective filtering and dynamic response. The selected values guaranteed stable operation of the converter and enabled the ADRC controller to maintain accurate voltage regulation under varying test conditions. The detailed values of the power stage components and test conditions are summarized in Table 4.3.

Table 4.3: Hardware implementation parameters of the Buck converter

Parameter	Symbol	Value
Inductance	L	1.6 mH
Capacitance	C	4500 μF
Load Resistance	R	24 Ω
Switching Frequency	f_{sw}	20 kHz
Input Voltage	V_{in}	24 V
Reference Voltage	V_{ref}	12 V

The experimental implementation uses the ADRC parameters that were previously computed based on a settling time of $T_{\text{settle}} = 0.02\,\text{s}$, as summarized in Table 3.2 in the preceding chapter 3 in section 3.2.3.

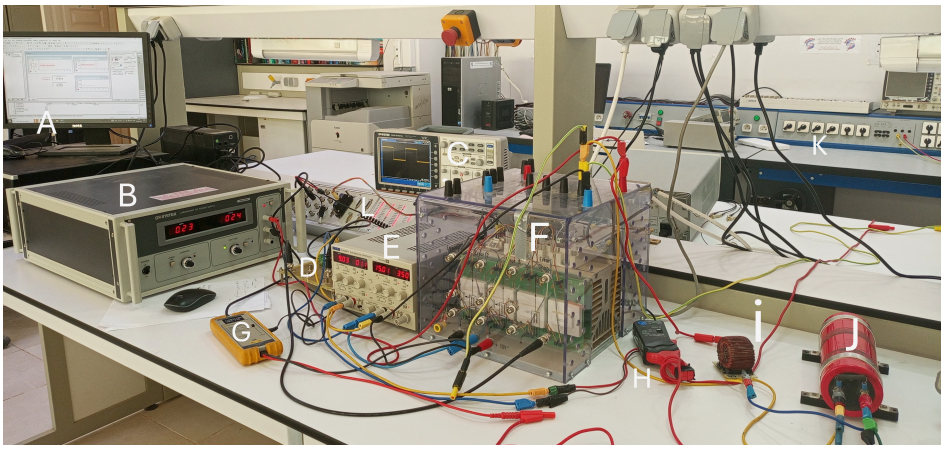


Figure 4.5: DC/DC Buck-converter experimental platform, with A- PC with control software, B-E- Input voltage DC, C- Oscilloscope , D- Driver Interface Board, F- IGPT half-bridge and G- Voltage sensor, H- Current sensor, i- Inductor, J- Capacitor, K- load, L- DSPACE controller, (K,J,i,F)- Buck-converter.

4.3.2 Experimental results for Buck-converter

Test Case 1: Input Voltage Disturbance with Two-Step Variation

In this experiment, the Buck converter was initially operated at a nominal input voltage of 12 V, with a stable duty cycle of approximately $D = 0.5$. To test the robustness of the ADRC controller, a two-step input disturbance was applied manually during real-time operation.
First, the input voltage was decreased, causing the controller to react by increasing the duty cycle to approximately $D = 0.94$, in order to maintain the desired output voltage. Then, the input voltage was sharply increased to approximately 30 V, resulting in a significant decrease in the duty cycle to about $D = 0.39$. Finally, the input voltage was returned to its original nominal value of 12 V.
Throughout the entire test, the load resistance and reference voltage were kept constant, and the controller was allowed to respond automatically to these input-side disturbances.

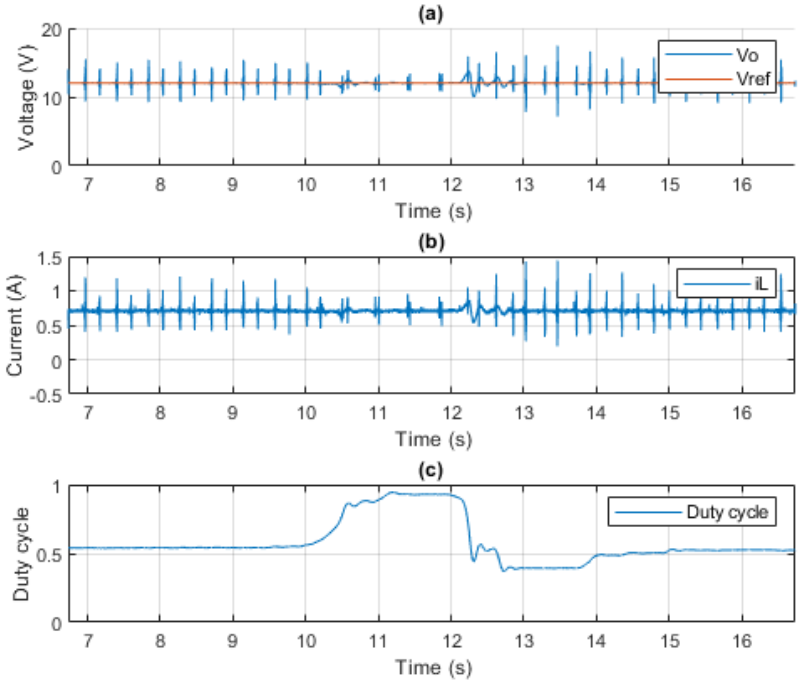


Figure 4.6: Exprimental of ADRC controller : System response to input voltage disturbance.

Experimental Result and Analysis

Figure 4.6. shows the system's response to the two-stage input disturbance. In subplot (a), the output voltage V_o experiences brief deviations during each disturbance but quickly returns to the reference V_{ref}. The ADRC controller demonstrates fast recovery and minimal overshoot in both cases.
Subplot (b) illustrates how the inductor current i_L adjusts dynamically to the changes in energy transfer caused by the input variation.
Subplot (c) clearly shows the duty cycle response: it increases to 0.94 during the input voltage drop, then decreases to 0.39 when the input voltage is raised to 30 V, and finally returns to its original level as the input is restored.
These results confirm the ADRC controller's strong ability to reject both sudden input voltage drops and rises, maintaining output stability through fast estimation and compensation via the Extended State Observer (ESO). The system remains stable throughout the test, with smooth transitions and effective regulation under real-time experimental conditions.

Test Case 2: Load Disturbance (Step Change in Resistance)

In this experiment, the Buck converter was tested under a load disturbance to evaluate the ADRC controller's ability to handle output-side variations. The system was initially operating under nominal conditions with an input voltage of 24 V and a load resistance of 24 Ω. During operation, the resistance was manually decreased to 12 Ω

to simulate a sudden increase in load current demand. The reference voltage and controller parameters remained unchanged during the test.

This disturbance was applied while monitoring the output voltage, inductor current, and duty cycle in real time using dSPACE ControlDesk.

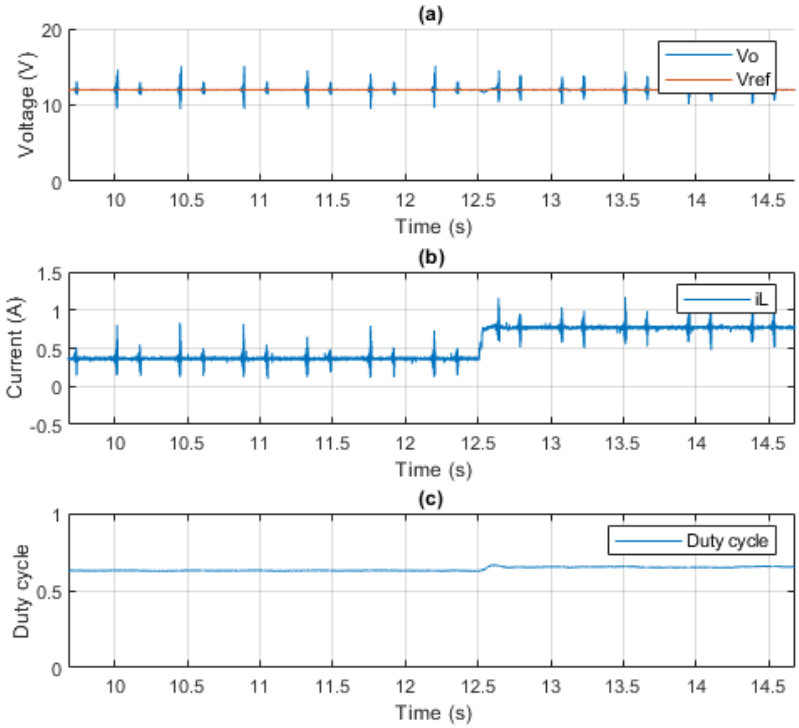


Figure 4.7: Exprimental of ADRC controller: System response to load disturbance.

Experimental Result and Analysis

Figure 4.7. presents the system's response to the load step change, As shown in subplot (a), the output voltage V_o remains well regulated despite the abrupt increase in load. Only a small and short deviation is observed, after which the voltage quickly returns to the reference V_{ref}.

In subplot (b), the inductor current i_L shows a clear step increase. Since the load resistance was halved, the output current approximately doubled, and the ADRC controller responded accordingly by adjusting the control signal to maintain stability and ensure sufficient energy delivery.

Subplot (c) illustrates the duty cycle behavior, which slightly increases in response to the increased current demand and settles quickly once the new steady-state is reached. This test confirms that the ADRC controller effectively compensates for load disturbances. By rapidly adjusting the control input based on real-time estimation of internal states and disturbances, the controller preserves system stability and ensures that the output voltage tracks the reference accurately under varying load conditions.

4.4 Conclusion

The experimental validation of the ADRC-controlled Buck converter, implemented on the dSPACE DS1104 platform, demonstrated strong agreement with the theoretical and simulation-based expectations. The real-time control setup—featuring accurate current and voltage sensing, efficient signal conditioning, and robust closed-loop feedback—enabled precise application of the ADRC algorithm using error-based modeling.

Experimental results under two distinct disturbance scenarios validate the effectiveness of the controller. During input voltage variations, the output voltage exhibited minimal overshoot and fast recovery, while the duty cycle adapted responsively to maintain regulation. In the load step test, the system showed excellent robustness, with the output voltage remaining stable despite significant changes in load demand. The ADRC's Extended State Observer (ESO) allowed the controller to rapidly estimate disturbances and adjust the control effort in real time.

Overall, the hardware results confirm that ADRC provides superior disturbance rejection, fast dynamic response, and reliable stability under varying conditions—making it a powerful control strategy for DC/DC converters in practical applications.

Appendix A

Symbols	**Description**
DC	direct current
ADRC	active disturbance rejection control
ESO	extended state observer
PID	Proportional–Integral–Derivative
PI	Proportional–Integra
PWM	pulse width modulation
V_in	input voltage of DC/DC converter
V_O	output voltage of DC/DC converter
I_L	inductor current
L	inductance value
C	capacitance value
R	resistive load
f_{sw}	switching frequency
T	switching period
d	duty cycle
d_s	disturbance
r	ADRC input reference
$\hat{z}$	estimated values of Error-based ADRC
f	total disturbance of the system
$\hat{f}$	estimated value of the total disturbance
b_0	system gain
$L_{1,2,3,11,12,21,22}$	gain of ESO

Table 4: List of Symbols and their Descriptions

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