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Field : … Electronic …
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Course Handout (Lectures)
Intended for students of: . Master. Level: ... 1st year...

# Semiconductor device fabrication processes

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# Foreword

This course material is part of the module "***Semiconductor Device Fabrication Processes***", intended for first-year students in the academic master's programme, specialising in "Microelectronics". This handout has been designed to enable students to learn about all the technological stages involved, detailing for each one the physical and chemical mechanisms at play, the precautions required and any constraints they may impose on other stages.

This fundamental module is worth 4 credits, with a coefficient of 2, and involves 3 hours of teaching per week, consisting of one lecture and one tutorial per week, and a total of 45 hours per semester.

This handout covers all the fundamental concepts involved in semiconductor device manufacturing processes. Beginning with a general overview of semiconductors and technological processes, the document is divided into seven chapters, each covering a specific topic.

First and foremost, this manuscript begins with a general overview of the main stages of semiconductor manufacturing.

The first chapter: **From sand to silicon wafer**: describes silicon purification, semiconductor pulling and growth, and wafer manufacturing.

The second chapter: **Epitaxy**: focuses on epitaxy techniques: molecular beam epitaxy, liquid phase epitaxy, and vapour phase epitaxy.

The third chapter : **Doping**: covers diffusion doping and ion implantation doping.

The fourth chapter, **Oxidation**, deals with dry oxidation and wet oxidation.

The fifth chapter, **Photolithography**, explains the principle of photolithography and different exposure techniques: contact, proximity, and projection.

**Etching and Chemical-Mechanical Polishing (CMP)** are covered in the sixth chapter.

Finally, in the seventh chapter, we conclude with **Metallization and Passivation**.

Each chapter includes a few exercises with fully detailed solutions.

Dr.Aissa Bellakhdar

# Chapter I : Generalities

## 1. Definition of microelectronics

Microelectronics involves the miniaturisation of increasingly complex electronic functions on a single medium (usually silicon).

Initially, the aim of microelectronics was to reduce the weight and size of devices, but these two criteria have become secondary to the improvement in reliability and reduction in cost that integration has brought about. For these various reasons, microelectronics is experiencing exceptional industrial growth, with production estimated to have doubled every year since 1963.

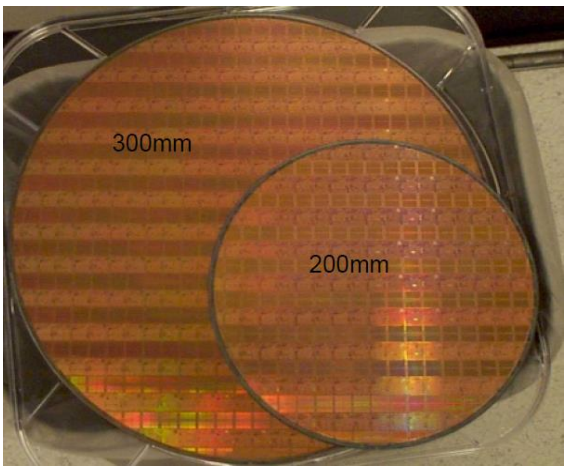



Fig I.1 300 mm and 200 mm silicon wafers

## 2. Brief history

- Since around 1920, industrial applications of electronics (known as T.S.F. at the time) have required a reduction in the weight and volume of devices.
- In 1947, the first bipolar transistor was developed by a research group at Bell Laboratories.
- In 1955, the transistor went into industrial production.
- Very quickly, various micro-assemblies of semiconductor devices were studied, leading in 1958 to the first integrated circuit, which contained a transistor, four diodes and a few resistors in a single silicon block.
- A year later, in 1959, Dr Noyce developed the planar method. Although initially developed for discrete circuits, this method can be considered the origin of the industrial development of integrated circuits.

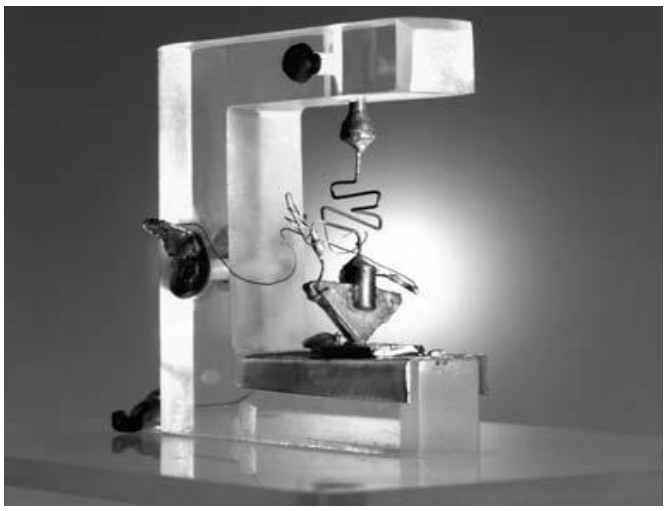


Fig. I.2 The first germanium bipolar transistor.Lucent Technologies Inc./ Bell Labs

## 3. Manufacture of semiconductor devices

### 3.1 What is a semiconductor?

A semiconductor is typically a crystalline material, often silicon, with electrical conductivity that falls between that of a conductor and an insulator. This device functions as a switch, controlling the flow of electrons within electronic systems. Modern technology relies heavily on semiconductors, which are used to manufacture chips, transistors, and diodes for computers, solar panels, and internet-connected devices.

**Semiconductor device manufacturing processes:** This refers to **the manufacture of semiconductor devices**, which encompasses the various operations involved in producing electronic components based on semiconductor materials. This category includes various types of components. A preliminary approach already allows us to differentiate between discrete components and integrated circuits (Wikipédia).

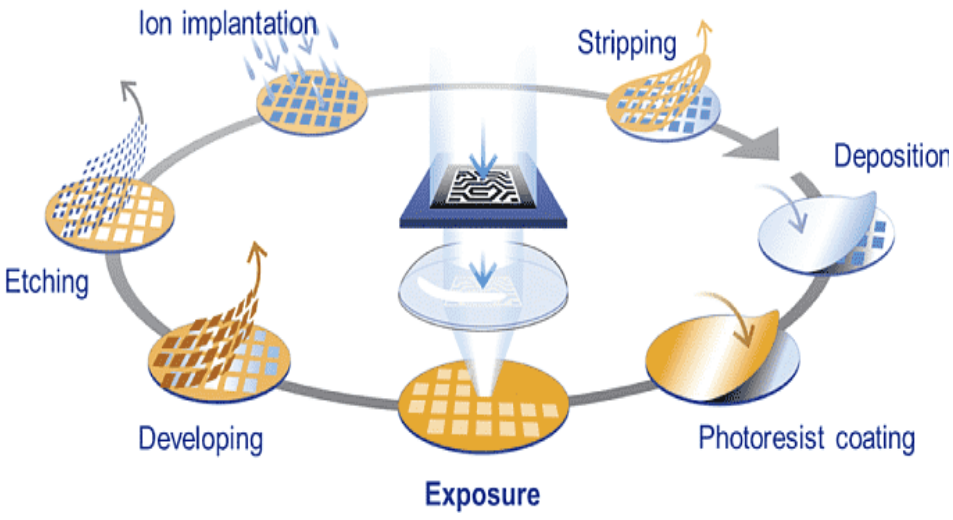



Fig I.3 manufacture of semiconductor devices

The development of semiconductor devices (integrated circuits, transistors) is a complex process carried out in clean rooms, transforming raw silicon into functional components via five key stages: material preparation, crystal growth (wafer), photolithography/etching for the pattern, doping, and metallization for interconnections. Planar technology is dominant, using deposition (epitaxy) and oxidation processes to build the component layer by layer.

### 3.2 Main Manufacturing Steps

- **Substrate preparation:** silicon is purified, crystallised (single crystal) and then cut into thin slices called wafers.
- **Oxidation:** Formation of a layer of silicon dioxide (Si) to insulate or protect the surface.
- **Photolithography:** transfer of circuit patterns onto the wafer using photosensitive resin and light (UV/DUV) to define the active areas.
- **Etching:** removal of unprotected materials using wet (chemical) or dry (plasma) methods.
- **Doping (ion implantation):** introduction of impurities (boron, phosphorus) to create P-type or N-type semiconductors.
- **Dépôt de couches minces :** ajout de matériaux conducteurs ou isolants (métallisation, épitaxie).

### 3.3 General information on processes

- **Planar technology:** components are manufactured on a flat surface through successive deposition and etching processes.
- **Environment:** manufacturing requires clean rooms, as even the smallest dust particle can destroy a circuit.
- **Types of doping:** P-type semiconductors are obtained by adding trivalent elements, and N-type semiconductors by adding pentavalent elements.
- **Back-end (end of process):** after manufacturing, the wafers are cut into individual chips, tested, and then encapsulated.

# Chapter II : From sand to silicon wafer

## II.1 Silicon purification :

- **Development of doped single-crystal ingots**
- **Preparation and characterization of substrates.**

Silicon is one of the most abundant elements in the Earth's crust. It is never found in its pure form, but rather as silica ($SiO_2$) or silicates.

Silicon, thanks to its high physical and chemical stability (in terms of temperature and oxidizing environments) and its natural protective layer ($SiO_2$), is the main material used in integrated circuit (IC) technology.

It is used in the form of single-crystal wafers, the preparation of which involves four main steps:

- Production of polycrystalline silicon (purification)
- Growth of Si single crystals
- Preparation of Si wafers;
- Wafer control

### 1. Production of polycrystalline silicon

### 1.1 Silica reduction: technical silicon

Since silica is not reduced by hydrogen, other reducing agents must be used:

- **Reduction by carbon (coke) in an electric arc furnace, 3000°C**

$$SiO_2 + C \rightarrow 2CO + Si$$

→ 97% pure silicon, with impurities: Fe, Cu, Al, B, Mg

- **Reduction by magnesium (violent reaction)**

$$SiO_2 + 2Mg \rightarrow 2MgO + Si$$

→ 99 % pure silicon

Technical silicon is not pure enough to be used in electronics. Chemical purification is therefore required, with the most commonly used process being preparation from trichlorosilane.

### 1.2 Preparation from trichlorosilane

Trichlorosilane is prepared from technical silicon, heated to 300°C, over which a stream of hydrochloric acid is passed:

$$Si + 3HCl \rightarrow SiHCl_3 + H_2$$

$SiHCl_3$ boils at 31.8°C; it is a highly flammable, non-toxic liquid that is easy to purify (by fractional distillation).

### 1.3 Reduction of trichlorosilane by hydrogen

$$SiHCl_3 + H_2 \overset{1100°C}{\rightarrow} Si + 3HCl$$

The silicon produced by the reaction is deposited onto a Si rod heated to 1100°C, which rotates to ensure uniform deposition. This produces very pure silicon (making physical purification unnecessary).

The resulting Si blocks, weighing several kilograms, are then:

- **Corrected** if they are to be drawn by floating zone (FZ),
- **Cut into pieces** if they are to be drawn using the Czochralski (CZ) method.

## II.2 Semiconductor production and growth

### Growth of Si single crystals

### 2.1 Czochralski method (CZ, 1917)

This is the most commonly used method.

- The Si pieces are placed in a high-purity quartz ($SiO_2$) crucible, which is itself placed in a graphite crucible.
- The whole assembly is melted in an inert atmosphere (argon) at approximately 1500°C.
- Heating is provided by high frequency (HF) or resistors (Si melting point: 1410°C).

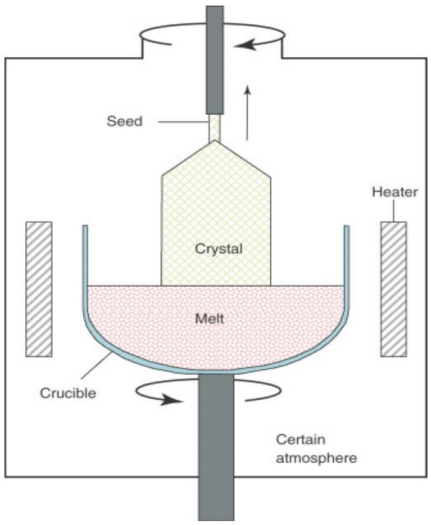



Fig. II.1 Schematic of the principle of the Cz method.

Fig. II. 3 Silicon crystal with a diameter of 300 mm and a weight exceeding 250 kg, grown by the Cz method.

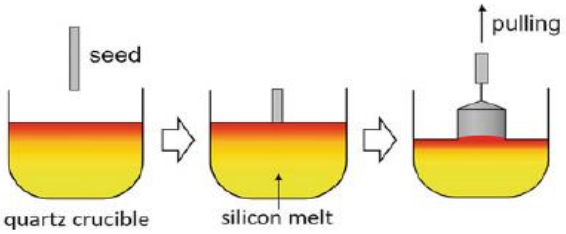



Fig.II. 2 A schematic of a CZ silicon crystal growth

**Doping:**

The doping agents (boron for p-type, phosphorus for n-type) are introduced into the bath:

- Either directly, after precise weighing,
- Either in powder form consisting of an "alloy grain" = Si doped to the solubility limit (β = 0.01 to 2 cm).

**Principle of the Czochralski method**

- Starting at 1500°C, the temperature is gradually lowered until crystallisation begins to occur on the surface of the bath → "zero supercooling" temperature (≈1415°C).
- A monocrystalline silicon seed (Ø 5 to 8 mm), suitably oriented (100) or (111), is attached to the end of the rotating extraction rod and lowered to the surface of the bath to "wet".
- The spiral pulling process is then carried out, producing a single-crystal ingot with the crystallographic orientation of the seed crystal.
- To homogenize the bath temperature, the crucible rotates in the opposite direction to the extraction rod.

### 2.1.1 Ingot drawing parameters

The extraction speed is set according to the "zero" point of the bath and the desired diameter of the ingot. It must remain less than or equal to the speed of crystallization of the liquid on the seed so that the liquid-solid interface remains fixed.

**Orders of magnitude:**

- Extraction speed: 1 to 5 mm/min
- Rod rotation speed (Z): 15 rpm
- Crucible speed (Δ): 10 rpm
- Mirror rise: 1.5 cm/k
- Ingot length: ~1 metre
- Diameter: 7.6 cm (3"), 100 mm (4"), 125 mm and even 150 mm.

**Uniformity of dopant addition**

The opposite direction of rotation of the rod and the crucible allows the bath to be homogenized. However, during crystal solidification, the concentration of the *Cs* solute (impurity trapped in the crystal) differs from that of the solute in the $C_l$ liquid. The ratio of the two concentrations is defined by the **segregation coefficient**:

$$k = \frac{C_s}{C_l} \qquad \text{(II.1)}$$

Table II.1 – Segregation Coefficient (k) for Dopants in Silicon

| Dopant | P | As | Sb | B | Al | Ga | In |
|---|---|---|---|---|---|---|---|
| k | 0.32 | 0.17 | 0.02 | 0.72 | 18.10 | $7.2\times10^{-3}$ | $3.6\times10^{-4}$ |
| Type | N | | | P | | | |

**Conséquences**

- For k < 1, the concentration of the dopant increases in the crucible ($Cs < C_l$) → non-uniform variation along the ingot.
- The resistivity of the crystal gradually decreases along the ingot (the crucible becomes enriched in solute).

Example: 76 cm ingot doped with phosphorus (P):

- Head: $\rho = 10\ \Omega \cdot cm$
- End: $\rho = 5\ \Omega \cdot cm$

**Remarks :**

- Boron has the highest k→ best concentration homogeneity.
- In microelectronics, this has little effect on a 300 µm wafer, but can be significant on a batch of 100 wafers.

### 2.2 Floating Zone (FZ) method

This method has an advantage over the Czochralski method: the molten zone is not contained in a crucible, which prevents $O_2$ contamination. It is used when high-resistance (> pure) silicon, intrinsic or undoped, is required.

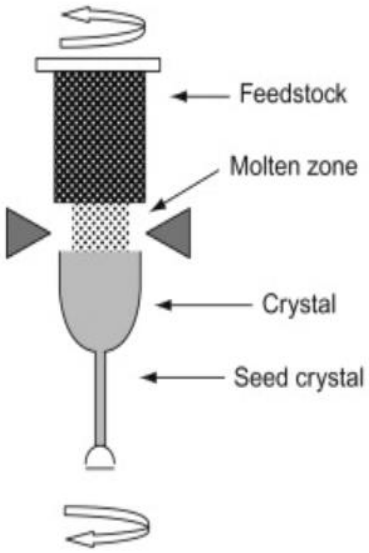



Fig. II**.** 4 Float-zone (FZ) apparatus for the growth of silicon single crystal.

**Principle of the device**

- A quartz tube contains a polycrystalline ingot 50 to 100 cm long, placed vertically.
- Neutral atmosphere (argon) or vacuum.
- For single crystal pulling:
  o the ingot is fixed at the top,
  o the seed is fixed at the bottom.
- An HF ring moves to melt the lower part of the ingot.
- The seed is brought into contact with the molten area, then removed with rotation (in the opposite direction to the ingot).

- The following are obtained in succession: a section with a small diameter, a conical section, then the final section.
- Unlike the CZ method, drawing is carried out from bottom to top.

The doping gases are fed into the quartz tube under controlled pressure. Temperature control is less critical than in the CZ method.

This technique is also used for the physical purification of polycrystalline Si (under high vacuum). Crystals with resistivities of up to 30,000 Ω·cm have been obtained. Ingots with a diameter of 76 mm (3") are cast, and with greater difficulty, 100 mm (4").

**Different methods of introducing the dopant:**

- Dopant distributed evenly throughout the initial polycrystalline material.
- If heavily doped, inserted into notches made on the surface of the polycrystalline material.
- Dopant introduced in gaseous form (most common method):
  o Hydrogen phosphine $PH_3$ (N type)
  o Hydrogen diborane $B_2H_6$ (P type)
- The dopant gases are mixed in the appropriate proportions with the inert gas.

### 2.2.1 Additional doping methods

**Solid and liquid dopants**

- **Heated solid dopant, swept by an inert gas:**
  - Phosphorus pentoxide $P_2O_5$ → N-type
  - Boron trioxide $B_2O_3$ → P-type
- Heated liquid dopant, whose vapours are carried away by the inert gas:
  - Phosphorus oxychloride $POCl_3$ → N-type
  - Boron tribromide $BBr_3$ → P-type

### 2.2.2 FZ method and dopant uniformity

The FZ method achieves greater chemical purity than the CZ method.

- CZ pulling involves a larger melt and a crucible, which increases the risk of contamination.
- FZ pulling is more sensitive to thermal gradients, but the introduction of the dopant in the gas phase ensures good axial uniformity.
- Radial uniformity depends on the rotation speed, which must be precisely adjusted.

**Result:** a crystal of high purity, not exposed to contamination by oxygen or carbon from the crucible. → No variation in resistivity during heat treatment.

### 2.2.3 Dislocation traces (linear defect)

- The dislocation density is higher than in CZ, as the molten zone is subject to stresses related to its weight.
- Typical values: $10^3$ to $10^5$ dislocations/cm².
- At the start of growth, the formation of the cone blocks the propagation of dislocations.

### 2.2.4 Comparaison CZ vs FZ

Below is a comparison between the CZ method and the FZ method.

Table II.2 – Comparison Between CZ and FZ Methods

| Criterion | CZ (Czochralski) | FZ (Floating Zone) |
|---|---|---|
| Maximum Diameter | 100 mm, 125 mm and more | 76 mm (above that, difficult) |
| Orientation | (100) and (111) | (100) and (111) |
| Normal Doping | Phosphorus (N), Boron (P) | Phosphorus (N), Boron (P) |
| Heavy Doping | Antimony or Arsenic ($N^+$) only | — |
| Applications | Integrated circuits, low-power devices, substrates | High resistivity: power detectors, transistors, PIN structures |

## 2.3 Another doping method: neutron transmutation

Phosphorus-doped silicon (n-type) can be obtained by transmutation.

- After cutting a Si ingot of the highest possible purity (FZ pull), the Si wafers are **bombarded with thermal neutrons** in a nuclear reactor.
- The atoms on the surface of the wafers are transmuted from Si to phosphorus, forming an n-doped zone.
- The resistivity and depth of this zone can be precisely controlled.

☞ This method produces uniformly doped Si crystals.

## II.3 Wafer manufacturing: final packaging of silicon

In microelectronics, the substrate (wafer) is the material on which monolithic circuits are integrated. It plays a dual role:

- Mechanical support
- Electrical functions

In order to reduce the cost of mass production of integrated circuits, the electronics industry has established international standards allowing for:

- Standardization of the materials used,
- Electrical and physical controls.

### 3.1 Preparation of the ingot

#### a - Grinding to the desired diameter

- Ingots with variations in diameter are reduced to standard sizes (Ø = 25, 50, 75 or 100 mm).
- Method: grinding followed by chemical etching (HF, $HNO_3$, $CH_3COOH$).
- Tolerance: defined Ø ± 0.1 mm.

#### b- Orientation – Machining the flat surface

- The orientation of each ingot is determined by X-ray diffraction (LAUE method).
- A flat surface is machined to mark this orientation.
- This flat surface serves as a reference for positioning the silicon wafer in all subsequent manufacturing stages, particularly cutting.
- Machining is performed using an abrasive wheel.

#### c- Machining the polarizing key

There is a code used to distinguish the crystallographic orientation and type of doping of the ingot (and therefore the substrates).

- Either a notch (key) or a smaller mark is made, the position of which characterises the wafer.
- Code (polished side at the bottom, mark at the bottom):
  - o (111) P type: no key (or small mark)
  - o (111) type N: 45° key (on the right)

o (100) type P: 90° key (on the left or right)

o (100) type N: 180° key (at the top)

**d- Bonding the ingot**

A bead of adhesive (avaldit) is applied to the ingot. This bead is used to secure the ingot when it is cut into discs.

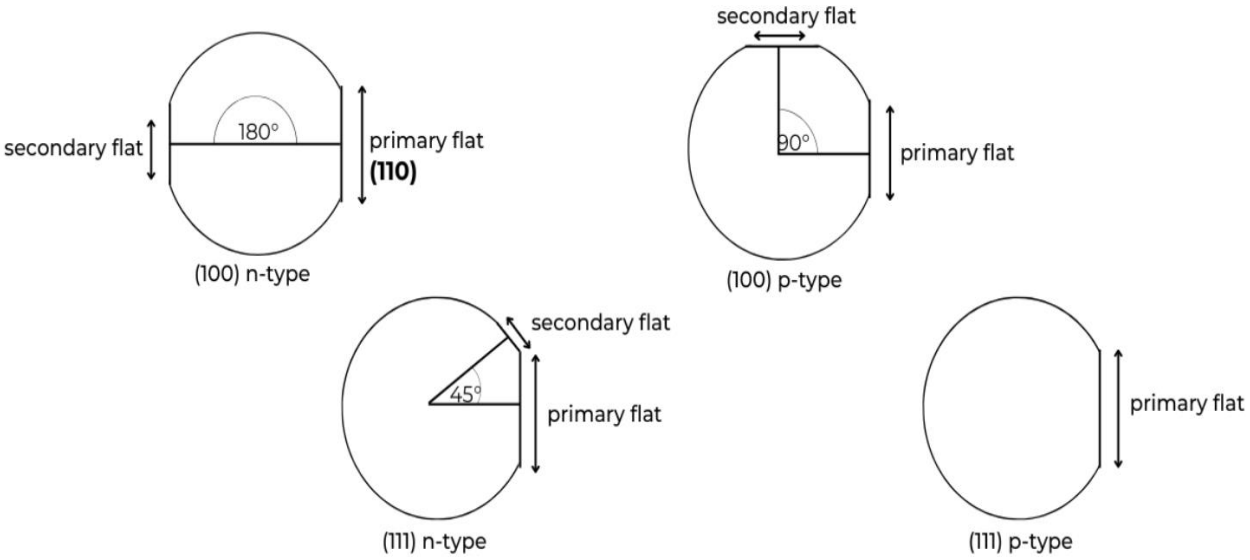



Fig II.5 : The standard orientation and identification flats for silicon wafers.

**3.2 Cutting the wafers**

The wafers are cut so that the surface is defined crystallographically with an accuracy better than 2°.

**a- Cutting with a ring saw**

- Rotation: 2,400 to 3,500 rpm
- Cooling: water
- Saw cut width: 250 to 300 µm

**b- Cutting with parallel (or multiple) blades**

- 25 to 50 wafers cut simultaneously
- Thickness: approximately 200 µm

**Thickness of wafers according to ingot diameter**

Table II.3 – Wafer Thickness by Ingot Diameter

| Ingot Diameter | Wafer Thickness (µm) |
|---|---|
| 76 mm (3") | 380 µm |
| 100 mm (4") | 500 µm |

**After cutting**

- Cleaning with a solvent (removes the glue)
- Sorting by thickness

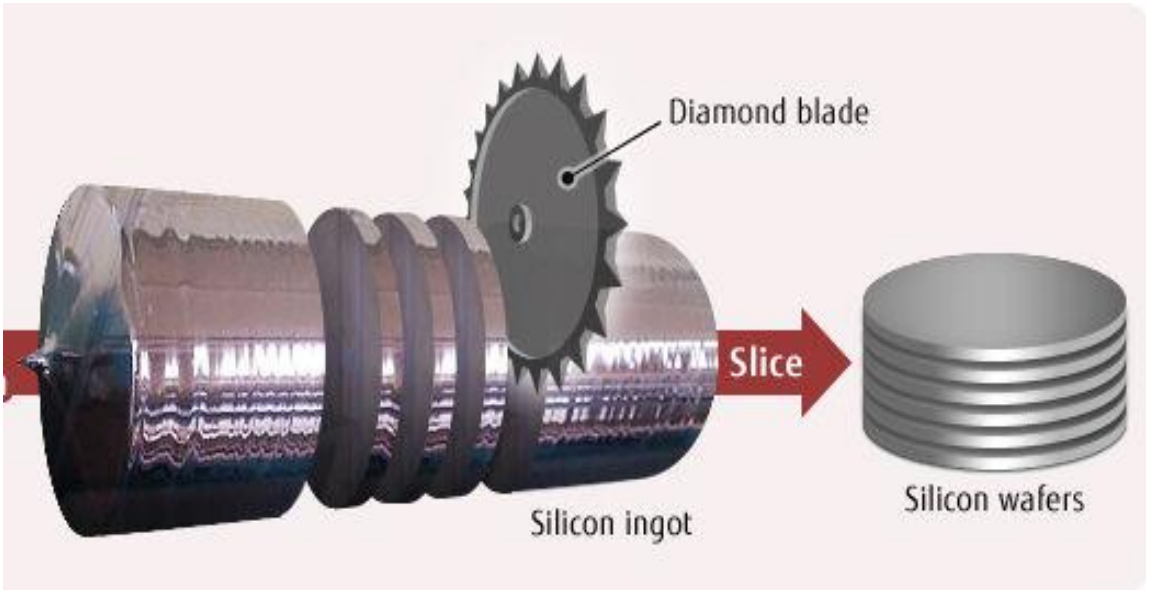



Fig II.6. Silicon wafers are processed by cutting boules into wafers

**3.3 Lapping of the plates – Polishing**

The dimensions of integrated circuits are a few µm and thin layers are < 1000 Å. It is therefore essential to eliminate surface irregularities that can cause structural defects.

- Mechanical lapping: on both sides (50 to 2 µm grains).
- Chemical lapping: etching bath ($HNO_3$ + HF, 5 to 10 min) + rinsing with deionised water.
- Mechanical-chemical polishing: applied to the upper surface of the wafers to obtain an optical polish.
  o Support: cast iron on cooled plate
  o Pressure: 0.5 kg/cm²

o Weakly chemically active solution (colloidal silicate) ⇒ Removal of all surface defects > a few tens of Å → optical polish.

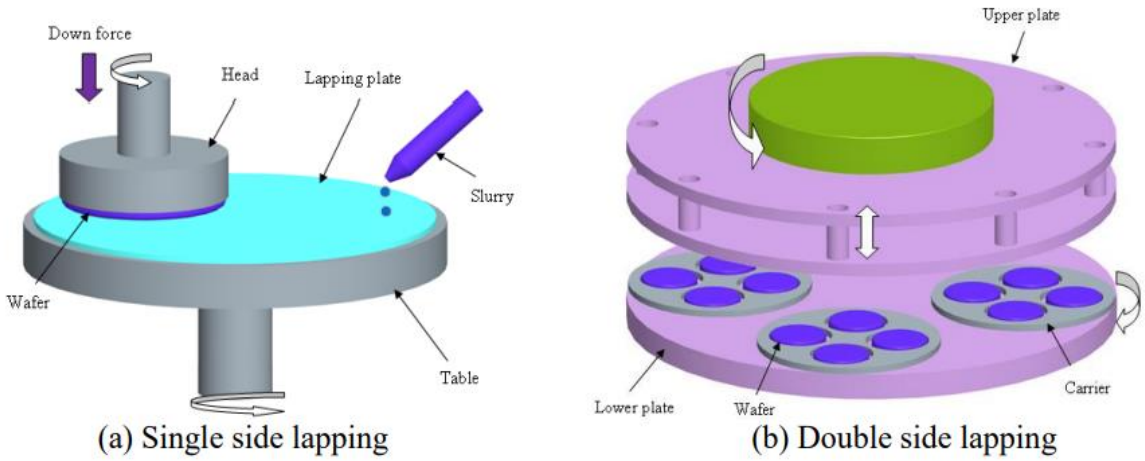



Fig II.7 Illustrations of lapping processes

### 3.4 Treatment of the rear side of the wafers

In order to remove any remaining impurities on the rear surface, impurity traps are created by welding or chemical etching, which makes it rough.

NB: there are optical polishing wafers on both sides.

### 3.5 Final cleaning

- Solvents and detergents
- Rinsing with deionised water
- Drying with nitrogen

The substrates are then examined under oblique illumination to detect any defects (holes, mechanical scratches).

## II.4 Wafer Control

### 4.1 Surface condition of the wafer

This is a very important factor, given the degree of precision required for photolithography masks. The following must be achieved:

- Ø 76 mm (3"): between 3 and 5 µm edge to edge
- Ø 100 mm (4"): less than 10 µm

### 4.2 Resistivity

The wafers have variable resistivity (ρ) depending on their position in the ingot, due to the segregation coefficient of the dopant, as well as radial variation. ☞ It is therefore necessary to control ρ.

#### 4.2.1 Resistivity measurement technique

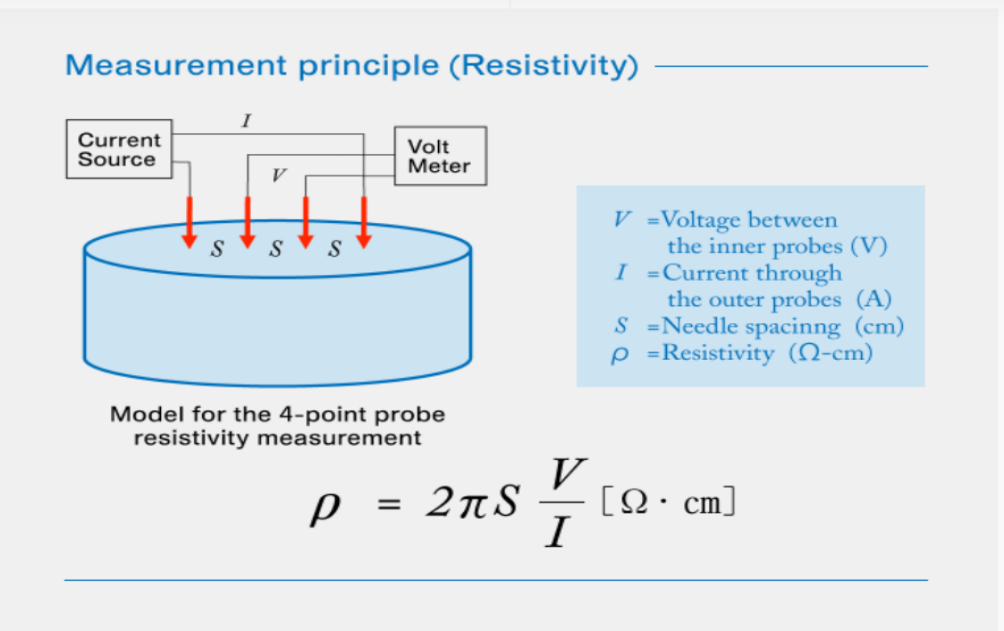



Fig II.8. Measurement principle (Resistivity)

The average resistivity $\bar{\rho}$ of wafers (as well as diffused or epitaxial layers) with a thickness $x_j$ is usually measured using the **four-point method**:

- Points spaced $S \approx 1\ mm$.
- A current I is applied between the outer points and the voltage V between the middle points is measured.

Formula: $$\bar{\rho} = 4.532 \cdot \frac{V}{I} \cdot x_j \qquad \text{(II.2)}$$

- $\bar{\rho}$ in $\Omega \cdot cm$
- $x_j$ in cm
- $V$ in volts
- $I$ in amperes

When the dimensions of the layers are not very large compared to $S$, a correction factor is applied.

**Square resistance : (Sheet Resistance)**

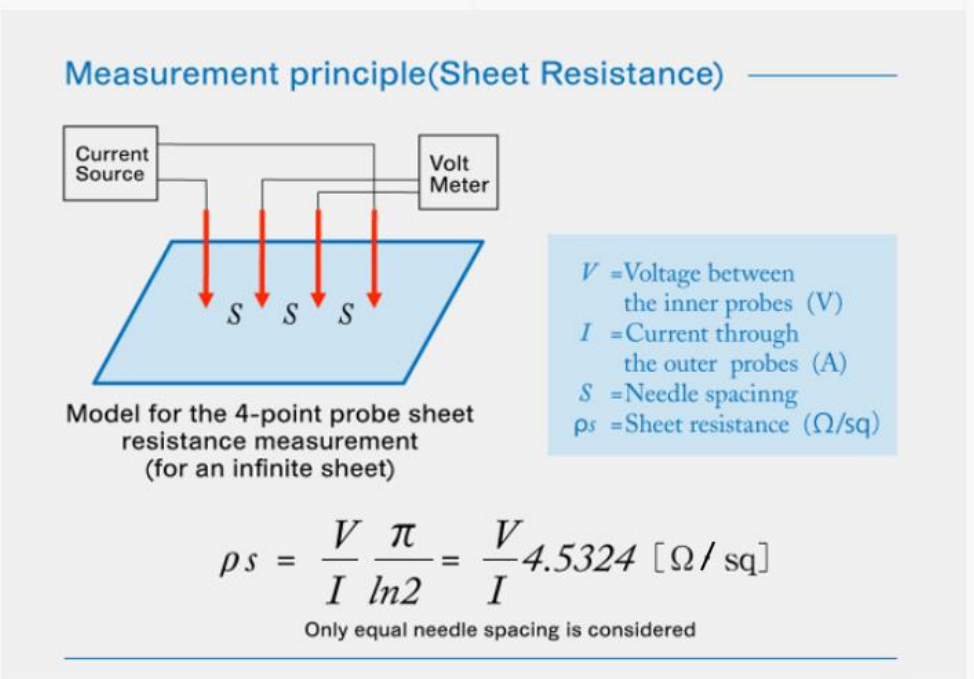
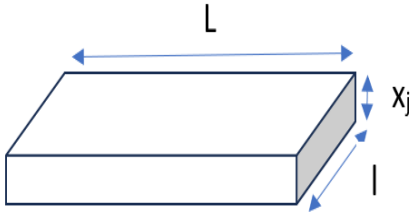



Fig. II.9 Measurement principle (Sheet Resistance)




$$R = \frac{\bar{\rho}}{x_j} \cdot \frac{L}{\ell} = R_0 \cdot \frac{L}{\ell} \qquad \text{(II.3)}$$

$R_0$: square resistance (resistance of a layer of thickness $x_j$), expressed in $\Omega/\text{sq}$.

**Note:** Some machines sort wafers according to thickness and $\bar{\rho}$.. The wafers are then sent to the workshops (clean rooms) in airtight boxes.

Each wafer is characterized by:

- Its diameter
- Its crystal orientation
- Its type (N or P)
- Its resistivity
- Its dislocation density
- Its thickness

### 4.2.2 Resistivity of wafers according to device type

Below is a wafer resistivity for different devices:

Table II.4 – Wafer Resistivity for Different Devices

| Resistivity Range (Ω·cm) | Devices |
|---|---|
| 0.001 – 0.5 | Zener diodes |
| 0.5 – 25 | Bipolar ICs, MOS-FETs, solar cells |
| 14 – 50 | Power transistors, HF transistors, diodes, rectifiers, thyristors |
| 40 – 100 | Diodes, rectifiers, avalanche diodes, thyristors |
| 100 – 1000 | High-power thyristors, high-voltage diodes, PIN diodes, detectors |

**Exercise 1** : Give the correct answer below; (The correct answer is in italics)

1. What is the chemical reduction equation of Silicion?

a. SiO + SiO2 ---> Si (solid) + SiO (gas) + CO (gas)

b. 3C + 2SiO2 ---> Si (solids) + SiO (gas) + 3CO (gas)

*c. SiC(solid) + SiO2 (solid) ---> Si (solid) + SiO (gas) + CO (gas)*

2. What is the chemical purity of silicon required for microelectronic grade material?

a. $10^{-7}$

*b.* $10^{-9}$

c. $10^{-12}$

d. $10^{-3}$

3. After electrolysis at high temperature, the Silicon purity is:

a. 95 %

b. 85 %

*c. 98 %*

d. 99 %

**Exercise 2:**

Using the Czochralski vertical pulling technique, a P-type silicon ingot is produced with a diameter of 5 inches, a length of 100 cm and a resistivity of 10 Ω·cm.

1- What is the mass of silicon that needs to be placed in the casting crucible, given that this charge is 1.5 times that of the ingot? To do this, calculate

a- The volume of the ingot;

b- The mass of the ingot;

c- Deduce the mass of silicon in the crucible.

2- Calculate the concentration of boron (B) and sodium (Na) in the ingot.

Given: 1 inch = 25 mm; density of silicon (Si): $\eta_{Si}$ = 2.34 g/cm³; µp = 460 cm²/V·s;

q (electron charge) = $1.6\times10^{-19}$ C.

**Solution 2:**

1 inche = 25 mm , diameter Φ = 5 inches , So, $R = \frac{5\ inches}{2} = \frac{125}{2} = 62.5\ mm$

L = 1m = 100 cm, the resistivity ρ = 10 Ω.cm

1- Calculating the mass of silicon to be placed in the crucible

a- volume of the ingot;

We calculate the volume of the ingot, which is a cylinder.:

$$v = \pi R^2 L = 3.14 \times (6.25)^2 (cm)^2 \times 100\ cm$$

$$v = 12265.62\ cm^3$$

b- The mass of the ingot;

To calculate the mass of silicon to be placed in the $M_{Si}$ crucible, we must first calculate the mass of the $M_L$ ingot.

The density of Si is η = 2.34g/cm³.

1 cm³ ⟹ 2.34 g/cm³

12265.62 cm³ ⟹ $M_L$

$$\Rightarrow M_L = 2.34\left(g/cm^3\right) \times 12265.62(cm^3) = 28701.55\ g$$

$$M_L = 28.7\ kg$$

c- Deduction of the mass of silicon in the crucible:

The mass of silicon to be placed in the $M_{Si}$ crucible is:

$$M_{Si} = 1.5 \times M_L = 1.5 \times 28.7\ kg = 43.05\ kg$$

2- Calculation of boron concentration : *Na*

the resistivity ρ = 10 Ω.cm , $\rho = \frac{1}{\sigma} = \frac{1}{q\mu_p N_a}$

$$N_a = \frac{1}{q\mu_p \rho} = \frac{1}{1.6\times10^{-19}\times460\times10} = 1.35 \times 10^{15}\ at.cm^{-3}$$

# Chapter III: Epitaxy

**Introduction:**

Epitaxy is a critical semiconductor production technology that involves growing a thin, high-purity single-crystal layer on top of a crystalline substrate while matching its orientation.

**III. 1- Definition : Etymologically:** 'epi' means '**on**' and "taxis" means '**arrangement**'.

Epitaxy is a technological process that involves growing crystal on crystal. The technique therefore consists of using the substrate as a crystal seed for growth and growing the layer by adding elements that make up the new layer. The epitaxial layer may be doped or undoped.

We will discuss, in the event that:

- the materials are identical, **homoepitaxy**; for example, epitaxy of an n-layer on an n+ layer, involved in the collector-base junction of a bipolar transistor, allowing better voltage resistance of this reverse-biased junction,

- the materials are different, **heteroepitaxy**; for example, growth of a layer of $Ga_xAl_{1-x}As$ on a layer of GaAs; this assembly enables the manufacture of superlattices or high-mobility layers for HEMT (High Electron Mobility Transistor) transistors.

In the latter case, growth will only be possible if there is lattice agreement, i.e. the same crystal lattice and very similar lattice parameters (slightly different distance between atoms for the new lattice; a maximum difference of around 1 to 2%).

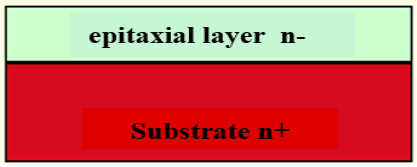



Fig III.1 Example of n-epitaxy on an n+ substrate; the substrate is said to be epitaxial.

The thin layer grown on the substrate is called an epitaxial layer. Figure 1 shows the growth of an epitaxial layer on the substrate.

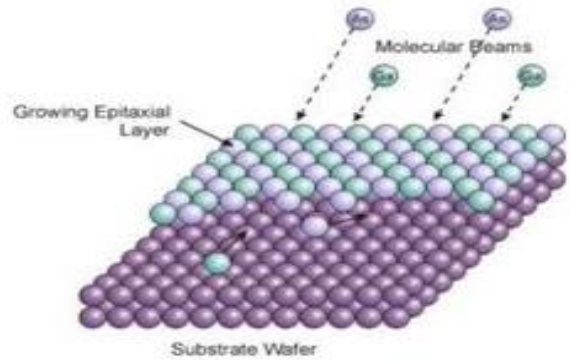



Fig III.2 MBE growth mechanism

Epitaxy is used to grow thin layers (a few nanometers thick).

**III. 2- Epitaxy techniques:**

There are several epitaxy techniques:

**2.1 Molecular beam epitaxy:** growth takes place under ultra-high vacuum. The elements to be deposited, contained in high-temperature crucibles, are evaporated and deposited by thermal transport onto the surface of the substrate, which is cooler but still hot enough to allow the atoms to move and rearrange themselves.

Molecular beam epitaxy (MBE) is a thermal evaporation method for depositing high-crystallinity thin films, essential in semiconductor preparation for electronic and optoelectronic devices and various nanostructured materials. Recognized as a fundamental tool in nanotechnology development, MBE offers flexibility as a growth technique.

The figure below illustrates the setup of a molecular beam epitaxy (MBE) system under ultrahigh vacuum. Effusion cells generate molecular beams directed toward the substrate, while the RHEED gun monitors surface structure during growth. The diagram highlights how controlled deposition enables fabrication of high-quality semiconductor thin films.

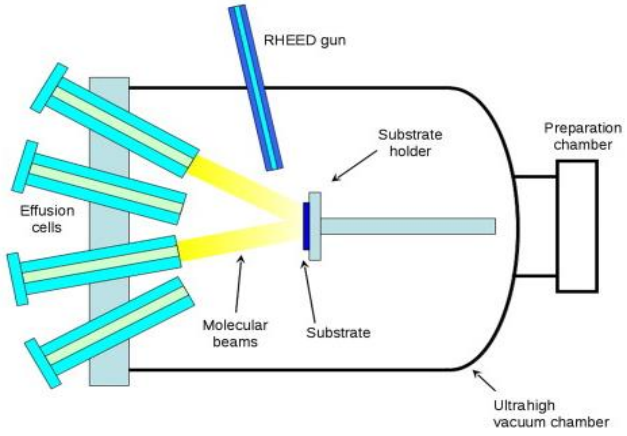



Fig III.3 Schematic of a typical system for molecular beam epitaxy (MBE).

**2.2 Liquid phase epitaxy:** Liquid phase epitaxy uses the principle of the Czochralski method. The substrate is brought into contact with a liquid phase supersaturated with the desired element, which precipitates and crystallises on the substrate. This technique has the advantage of being fast, but it is less precise than vapour phase epitaxy.

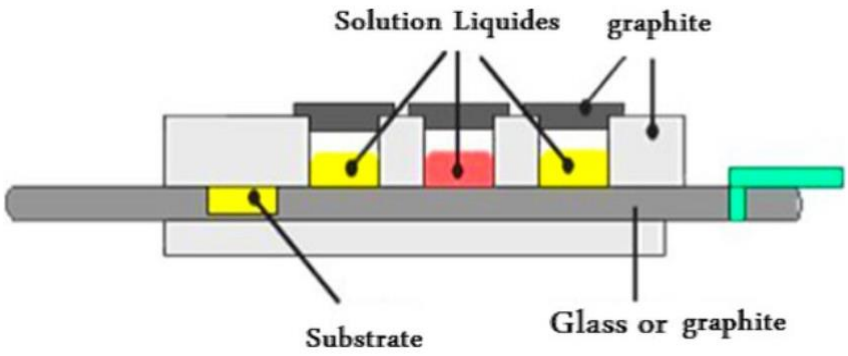



Fig. III.4 liquid phase epitaxy technology

**2.3 Vapor phase epitaxy:** the technique of depositing thin layers by vapour phase epitaxy (VPE or chemical vapour deposition, CVD) is widely used for silicon. For an epitaxial layer to be deposited, two conditions must be met. The first is that the atoms must find a place where they can lose their excess energy; these places are called nucleation sites. The second is that these atoms must find a site in the lattice to accommodate them.

Vapor phase epitaxy (VPE) involves the growth of monocrystalline semiconductor layers on substrates using organometallic compounds under low pressure. Initially developed for silicon and gallium arsenide, VPE now applies to a wide range of semiconductor materials in micro- and optoelectronics. The process includes a vapor mixture entering a reactor where substrates are positioned. For silicon, key components are silicon tetrachloride ($SiCl_4$) or silane ($SiH_4$); for arsenides and phosphides, it involves metal alkyls, arsine ($AsH_3$), and phosphine ($PH_3$). The vapor decomposes at high temperatures, leading to layer-by-layer deposition of semiconductor compounds. This technique is crucial for creating GaAlAs/GaAs heterostructures, quantum wells for injection lasers, and GaN-based materials for LEDs and short-wavelength lasers.

This figure presents the design of a vapor phase epitaxy (VPE) reactor. It highlights the arrangement of gas inlets, reaction chamber, and substrate positioning for controlled film growth. The schematic emphasizes how reactor geometry ensures uniform deposition of epitaxial layers.

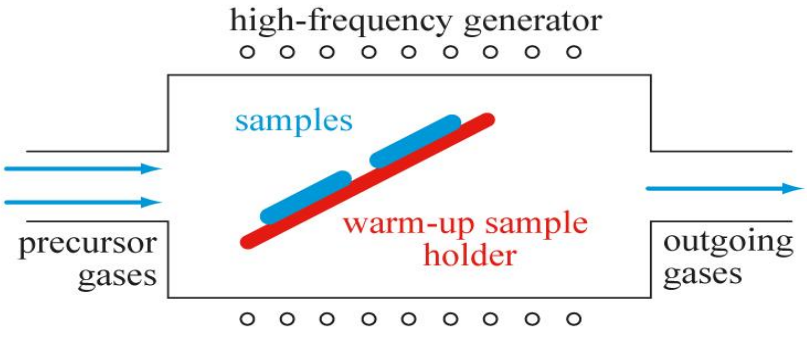



Fig. III.5 Vapor phase epitaxy unit reactor design

Several processes for silicon epitaxy are available in function of the silicon gas sources that can be $SiCl_4$,$SiHCl_3$, $SiH_2Cl_2$, or $SiH_4$.

1) from tetrachlorosilane, $SiCl_4$, the reaction is:

$$SiCl_{4\ gaz} + 2H_{2\ gaz} \rightleftharpoons Si_{sol} + 4HCl_{gaz}$$

This reactio is usually performed at a temperature about 1250°C that leads a high doping redistribution during this step.

2) from trichlorosilane, $SiHCl_3$, the reaction is :

$$SiHCl_{3\ gaz} + H_{2\ gaz} \rightleftharpoons Si_{sol} + 3HCl_{gaz}$$

It occurs usually at a temperature close to 1100°C; this is the most industrially used technique presently.

3) from the pyrolyze of dichlorosilane, $SiH_2Cl_2$ , the reaction is :

$$SiH_2\ Cl_{2\ gaz} \rightleftharpoons Si_{sol} + 2HCl_{gaz}$$

This reaction leads to a good quality of the crystal with a high enough deposition rate.

The three presented techniques have however the disadvantage to involve chloride acid that can react with silicon surface and depending on the physical parameters can etch the crystal instead to grow the crystal. In order to well control this problem, the partial pression of this HCl gas is one of the main parameters of the process.

4) from silane, $SiH_4$ :

The pyrolyze reaction of silane is a non-reversible reaction:

$$SiH_{4\ gaz} \rightarrow Si_{sol} + 2H_{2\ gaz}$$

This reaction occurs at 1000°C without chloride compounds. This technique Callows to fabricate abrupt junctions because the temperature is rather low in comparison with the other technique ‘ones, but the silane gas is expensive and dangerous (it burns instantaneously in the free atmosphere) and the deposition rate is low.

**Exercise:** Give the correct answer below; (The correct answer is in italics)

1. The typical growth rate of molecular beam epitaxy is:

a. a few micrometres per minute

b. a few centimetres per minute

c. *a few nanometres per minute*

d. a few picometres per minute

2. Homoepitaxy corresponds to the growth of:

a. two different materials with the same lattice parameter

b. *the same material doped differently*

c. materials with different lattice parameters

d. a single material doped uniformly

3. The positioning of atoms during growth occurs preferentially:

a. *in free crystalline sites located in the first atomic layer*

b. on the surface of the layer

c. at crystal defects

d. on step edges on the surface

# Chapter IV : Doping

Doping is a technique that involves introducing suitable impurities into the material in controlled quantities, which has the effect of increasing its conductivity. In N-type (negative) semiconductors, conductivity is provided by free valence electrons (as in metals), and the dopants are As, Sb, P, etc. in P-type (positive) semiconductors, conduction is provided by free holes (a hole being equivalent to an absence of electrons), and the dopants are B, Al, Ga, In, etc. The concentration of doping impurities allows the conductivity of the semiconductor to be controlled very precisely.

## IV.1 Diffusion doping

### 1- Diffusion phenomenon:

Diffusion is a very common phenomenon in nature, corresponding to the tendency of species, particles, atoms or molecules to spread out due to energy excitation caused by heat. Depending on the medium in which these species move, the spread will be greater or lesser. At room temperature, the phenomenon of diffusion will be very significant in a gaseous medium, weaker in a liquid medium and practically non-existent in a solid medium. To achieve diffusion in a solid or crystal, the material must be heated to temperatures close to 1000°C.

### 2- Atomic-scale diffusion mechanism:

The diffusion mechanisms involved in a crystal depend on the nature of the crystal and the nature of the diffusing species. It should be noted that the atoms constituting the crystal can themselves diffuse; this is referred to as the self-diffusion mechanism. Self-diffusion is important because it allows vacancies to be created in the crystal lattice.

Diffusion in solids can be considered to be due to point defects in solids.

In a solid, a given atom can acquire kinetic energy greater than the average energy of the atoms in the lattice and can thus ‘jump’ to another position. This jump may allow it to occupy the place of another atom absent from the lattice, i.e. it occupies a vacancy, or it may allow it to insert itself into the space between atoms that are well arranged in the lattice, i.e. in an interstitial position (Fig IV.1).

An atom that leaves its place in the lattice to occupy a neighbouring interstice creates what is known as a Frenkel defect. The gap formed by the detachment of an atom from the surface of the solid, which diffuses inwards, creates what is known as a Schottky defect.

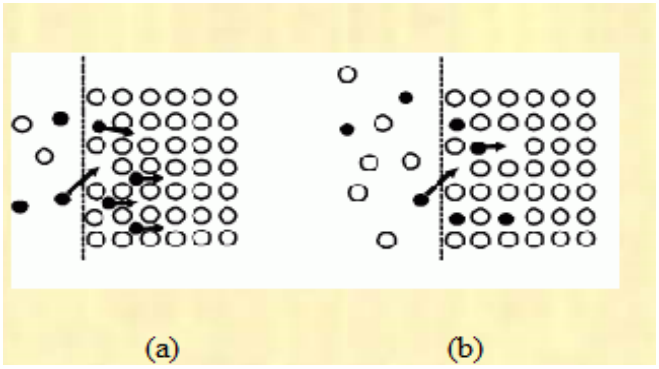



Fig IV.1 Mechanisms of impurity diffusion in a semiconductor crystal, (a) through the generation of interstitial atoms, (b) through the generation of vacancies.

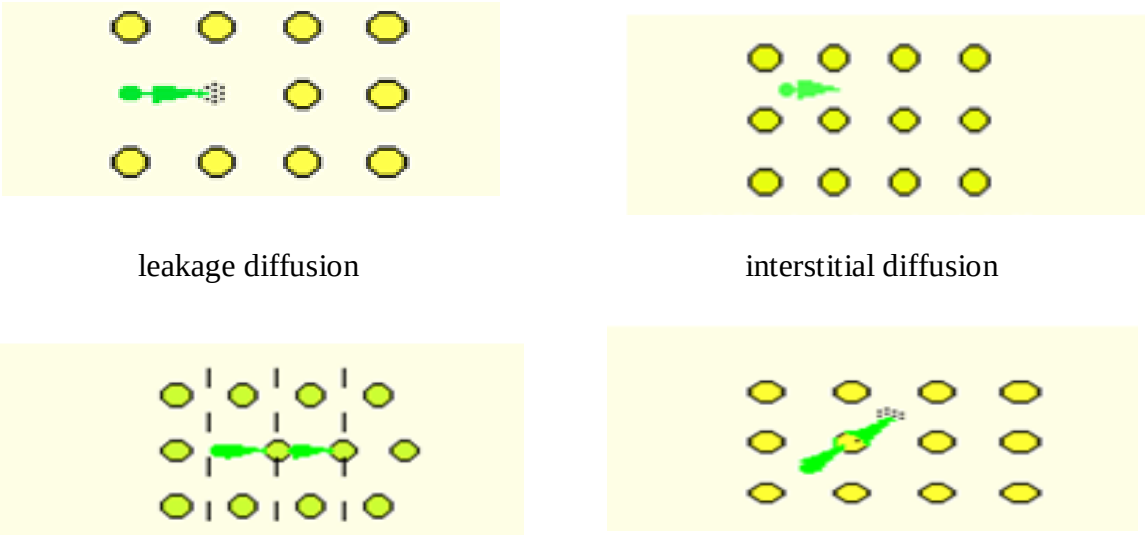



Fig IV.2 Diffusion mechanisms at the atomic scale. These mechanisms will differ depending on the nature of the diffusing species and the crystal.

**3- Diffusion equations :**

**Fick's first law** describes the tendency towards diffusion; the flow of atoms is proportional to the concentration gradient of these atoms and is expressed as:

$$J = -D\frac{\partial C(x,t)}{\partial x} \qquad \text{(IV.1)}$$

*D* is the diffusion coefficient.

The diffusion coefficient *D* is a constant that characterizes the speed at which diffusion occurs. It is related to the mobility of impurities by Einstein's relation:

$$\frac{D}{\mu} = \frac{kT}{q} \qquad \text{(IV.2)}$$

*D* depends heavily on temperature; almost zero at room temperature, this coefficient is of the order of unity in square microns per hour for temperatures of around 1100°C.

The dependence of *D* on temperature is of the form:

$$D = D_0 exp^{\frac{-E_a}{kT}} \qquad \text{(IV.3)}$$

where $E_a$ is the activation energy and k is Boltzmann's constant. $D_0$ is called the pre-exponential coefficient; it depends on the semiconductor and the impurity.

**The second Fick's law** to consider is the continuity equation. In a given volume element with thickness dx, if the incoming flux is greater than the outgoing flux, the concentration of the species in question increases. This equation is also used for electron and hole carriers in a semiconductor, but in the case of atoms there is neither generation nor recombination.

$$\frac{\partial C(x,t)}{\partial t} = \frac{\partial J(x,t)}{\partial x} \qquad \text{(IV.4)}$$

Combining the two previous equations leads to the following second Fick's law:

$$\frac{\partial C(x,t)}{\partial t} = \frac{\partial}{\partial x}\left(\frac{\partial C(x,t)}{\partial x}\right) = D\frac{\partial^2 C(x,t)}{\partial x^2} \qquad ; D\ (\text{cm}^2/\text{s}) \qquad \text{(IV.5)}$$

To integrate this differential equation, which involves a derivative with respect to time and a double derivative with respect to space, three specific conditions (or limits) must be determined. These conditions will depend on the technological process used.

**4- Diffusion processes:**

The diffusion processes will depend on the nature of the dopant sources. There are three main types of sources that can be used to supply the dopant elements that need to be introduced into the substrates. These sources are **gaseous, liquid** or **solid**.

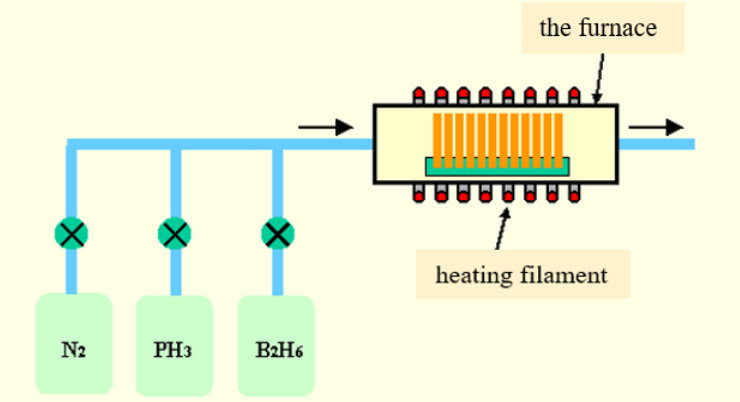



Fig IV.3 Diffusion in a furnace from gaseous sources. The dopant gases are carried by a neutral carrier gas, such as nitrogen.

Gaseous sources are gases such as arsine, $AsH_3$, phosphine, $PH_3$, or diborane, $B_2H_6$ (figure above). Note that a neutral gas (nitrogen) circulates continuously to prevent contamination by elements from the ambient atmosphere. This nitrogen must be very pure so as not to contaminate the furnace.

Liquid sources such as $POCl_3$ or $BBr_3$ are preferred, as they are liquid at room temperature but can be easily vaporised for introduction into diffusion furnaces (fig IV.4).

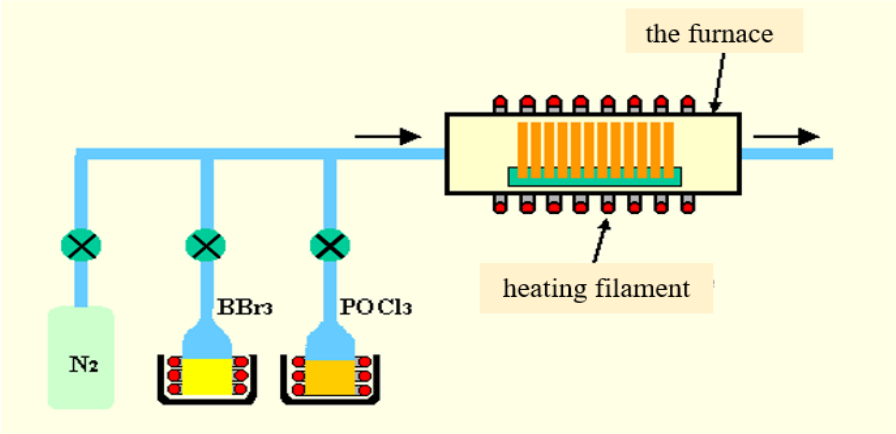
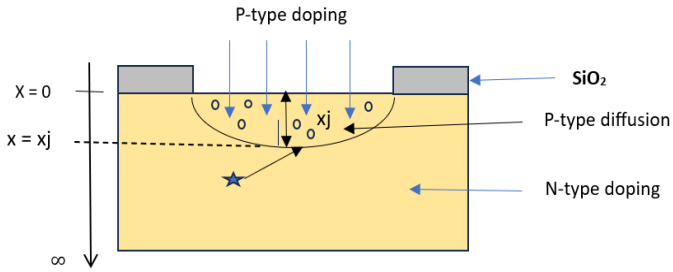



Fig IV.4 Diffusion from liquid sources. The flasks containing the liquids are heated to vaporise the liquid so that it can enter the furnace.

| | **Deposition or pre-deposition stage** | **Drive-in diffusion step** |
|---|---|---|
| **Diffusion process steps** | • The dopant diffuses to a depth of approximately 1/10 µm when the furnace is heated to a temperature of 1000 °C for a period of time t = 60 minutes.<br>• During this stage, a layer of silica glass doped with phosphorus oxide ($P_2O_5$) or boron oxide ($B_2O_3$) is formed. | During this stage:<br>• We are stopping the introduction of doping substances.<br>• The doped substrates are subjected to heat treatment in a neutral atmosphere to allow the dopants to penetrate more deeply. |
| **Doping profile** | $$N(x) = N_S erfc\left(\frac{x}{2\sqrt{Dt}}\right)$$<br>Ns is the concentration on the surface equal to the solubility limit of the impurity at the diffusion temperature.<br>Dans In this expression, the erfc function represents the complementary error function defined by the expression:<br>$$erfc(x) = \frac{2}{\sqrt{\pi}}\int_Z^{\infty} e^{-t^2}dt$$ | • In this step, the doping profile is given by:<br>$$N(x) = \frac{Q}{\sqrt{\pi Dt}} e^{-}\frac{x^2}{4Dt}$$<br>• Q is the total amount of impurities (atoms/cm²).<br>• The doping profile is therefore Gaussian. |

**Diffusion in silicon – modelling and implementation**

## 1. Diffusion modelling




Consider P-type diffusion in an N-type substrate. The diffusion depth xj corresponds to the junction depth.

On the surface, diffusion occurs to $0 \leq x \leq x_j$

In N-type doping (the concentration $N_D$ = the initial concentration of $C_B$ deposit).

At point xj (point ★), the concentration of type P = the concentration of type N

xj is: Diffusion depth = junction depth

The solution of Fick's two laws allows the concentration C(x,t) to be determined. In the case of pre-deposition, the boundary conditions are:

1) At t = 0: C(x,0) = 0 for all x.

2) At the surface (x = 0): C(0,t) = Cs (constant concentration).

3) For x → ∞: C(∞,t) = 0 (limited diffusion).

The solution to the diffusion equation is:

$$C(x,t) = C_s \, erfc\left(\frac{x}{2\sqrt{(Dt)}}\right) \qquad \text{(IV.6)}$$

The junction depth $x_j$ is obtained when $C(x_j, t) = C_B$:

$$x_j = 2\sqrt{(Dt)}\, erfc^{-1}\left(\frac{C_B}{C_S}\right) \qquad \text{(IV.7)}$$

## 2. Drive-in diffusion step

After the pre-deposition stage, the source of impurities is removed. The impurities then diffuse into the substrate: this is the redistribution stage.

## 3. Practical diffusion process

The silicon wafers are placed in a furnace heated to a high temperature, generally between 800°C and 1200°C.

The system comprises:

• A main furnace containing silicon wafers.

• A source furnace containing doping impurities.

**Principle:** Impurities are heated to their melting or evaporation temperature. They are then transported to the main furnace using a neutral gas, usually nitrogen ($N_2$), called a carrier gas.

In practice, the pre-deposition and drive-in diffusion steps can be carried out in the same furnace. The duration and temperature of redistribution are often higher than those of pre-deposition.

## IV.2 Ion implantation doping

### 1- Introduction:

Ion implantation has long been used in the electronics industry.

The idea came from Shockley (one of the inventors of the transistor), who proposed ion implantation for doping semiconductors as early as 1951. From 1971 onwards, the process was industrialized for the manufacture of integrated circuits. Proposed in 1973 for mechanical applications, it was quickly put to successful use. Applications emerged in the mechanical, aeronautical and biomedical industries.

### 2- Definition:

Ion implantation is a materials engineering process. As its name suggests, it is used to implant ions from one material into another solid, thereby changing the physical properties of that solid.

Ion implantation is used in the manufacture of semiconductor devices, for the surface treatment of metals, and for research in materials science. Ions can be used to change both the chemical properties of the target and its structural properties, as the crystalline structure of the target can be damaged or even destroyed.

This process involves introducing ionised projectile atoms with sufficient energy to penetrate the target sample (usually a wafer). This penetration only occurs in surface areas. This process is mainly used to dope semiconductors during device manufacturing (creation of source or drain areas in a MOS transistor, a base and an emitter in a bipolar transistor, etc…). The doping atoms are generally: B, P, As, In, etc…

The energies of ionised atoms can range from 3 keV to 500 keV.

Depending on the nature of the implanted material, the nature of the accelerated ion and the acceleration energy, the average penetration depth can range from 100 Å to 1 µm.

Indeed, a rough calculation shows that approximately one hundred electron volts are lost per atomic layer (approximately 2.5 Å).

**3- Advantages of this technique:**

It allows precise control of the total quantity of atoms implanted (implantation dose) and the concentration profile of the dopant. This precision allows, in particular, the adjustment of the current gain value of a bipolar transistor or the adjustment of the threshold voltage of a MOS transistor (choice of transistor type – enrichment or depletion). It should be noted that this process is carried out in a vacuum and therefore in a dry atmosphere.

**4- Disadvantages of this technique:**

The bombardment of a single crystal by atoms causes damage to the implanted crystal structure. It is therefore necessary to restore the crystallinity of the material; this is achieved by thermal annealing. Thermal annealing also allows the dopant atoms to be redistributed, thereby modifying the doping profile through diffusion. It should be noted that this annealing can also activate the implanted dopant (transition to a substitution site).

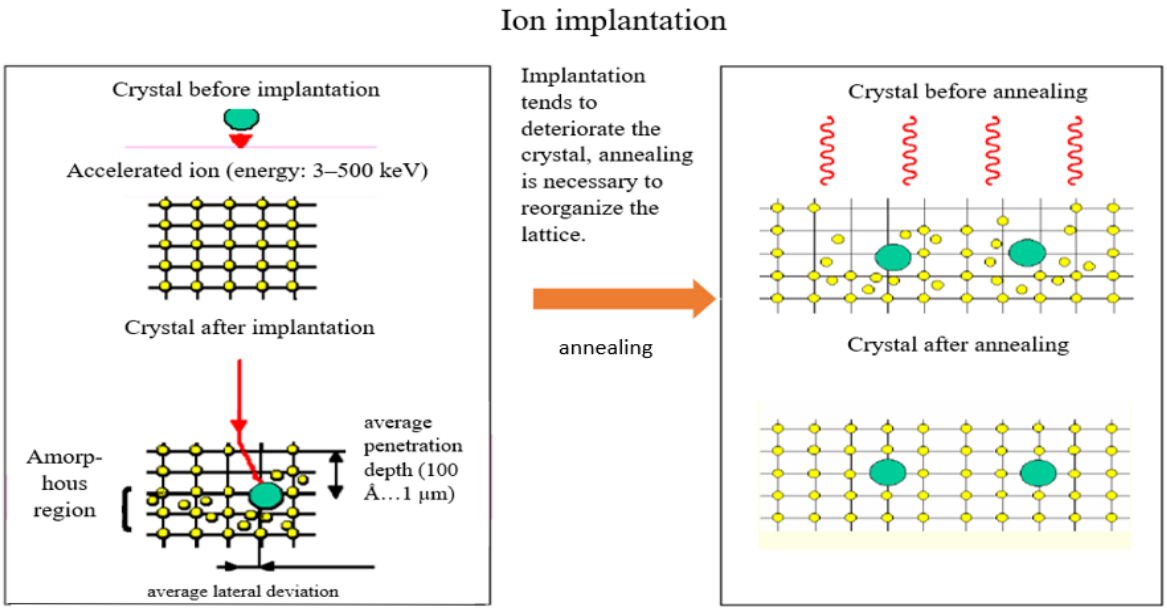



Fig IV.5 damage to the implanted crystal structure

**5- The ion implanter:**

The ion implanter is essentially an ion accelerator.

The figure below shows a schematic diagram of an ion implantation system. Ions are formed from source atoms and accelerated through an ion beam analyzer that selectively allows desired ions to pass based on their mass, charge, velocity, and magnetic field intensity. The resulting ion beam is shaped using electrostatic and magnetic lenses for substrate scanning. Ion implantation offers precise control over implantation depth (10–100 keV depending on acceleration voltage) and ion dose, which is monitored via ion current. A patterned silicon dioxide

layer serves as masking, and annealing is required afterward to reconstruct the silicon crystal lattice and incorporate the implanted atoms.

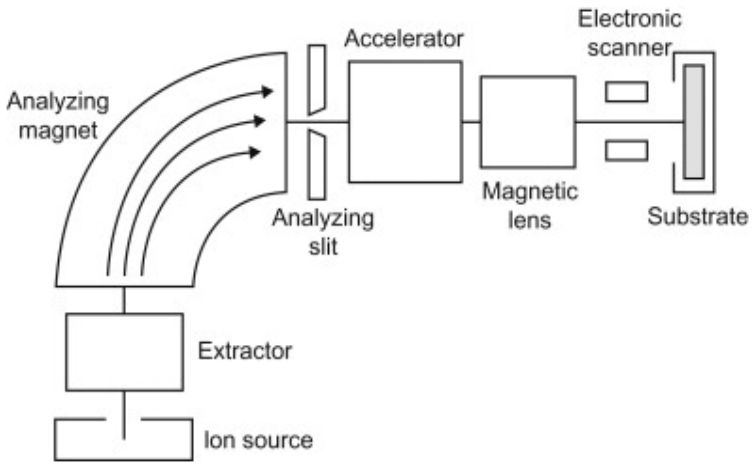



Fig IV.6 Schematic of a typical ion implanter.

Heavy, electrically charged incident ions lose their energy either through collision with the nuclei of the solid substrate or through interaction with electrons in the solid. The mechanism of energy loss depends on the atomic number of the ion and its energy. This mechanism is dominated by interaction with nuclei for ions with a large atomic number Z and low energy E, and by interaction with electrons in the solid for ions with a small Z and high energy E.

The penetration depth of ions has a Gaussian distribution. The figure below (Fig.IV.7) shows this distribution and its spread for ions heavier and lighter than the substrate. In a single crystal, this depth also depends on the orientation of the crystal.

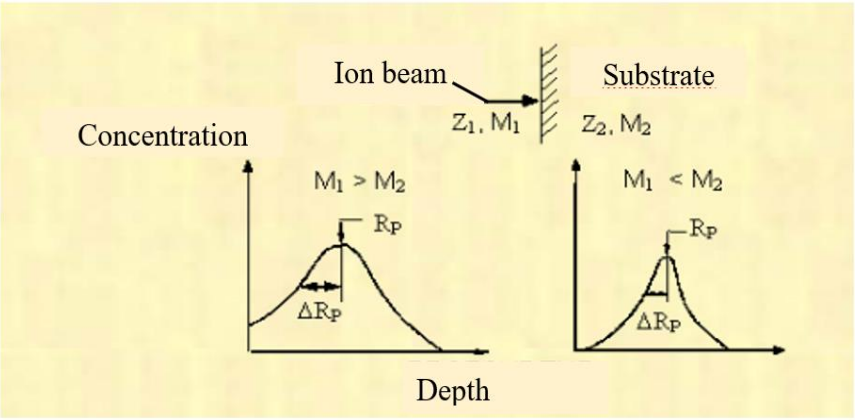



Fig IV.7 Distribution of ions implanted in an amorphous target for M1>M2 and for M1< M2. As a first approximation, the depth depends on the mass of ion M1 and its incident energy, while the relative spread ΔRp/Rp depends on the ratio M1/M2.

**6- Concentration profile:**

The incident ions lose energy through successive collisions with the atoms in the crystal lattice. This explains both the dispersion of trajectories and the statistical definition of an average penetration depth. The most appropriate statistical model is Gaussian. We thus define two parameters:

– the average penetration depth (range): $R_P$, with a standard deviation $\Delta R_P$.

– the average lateral deviation (perpendicular to the implantation direction), $\Delta R_p^+$.

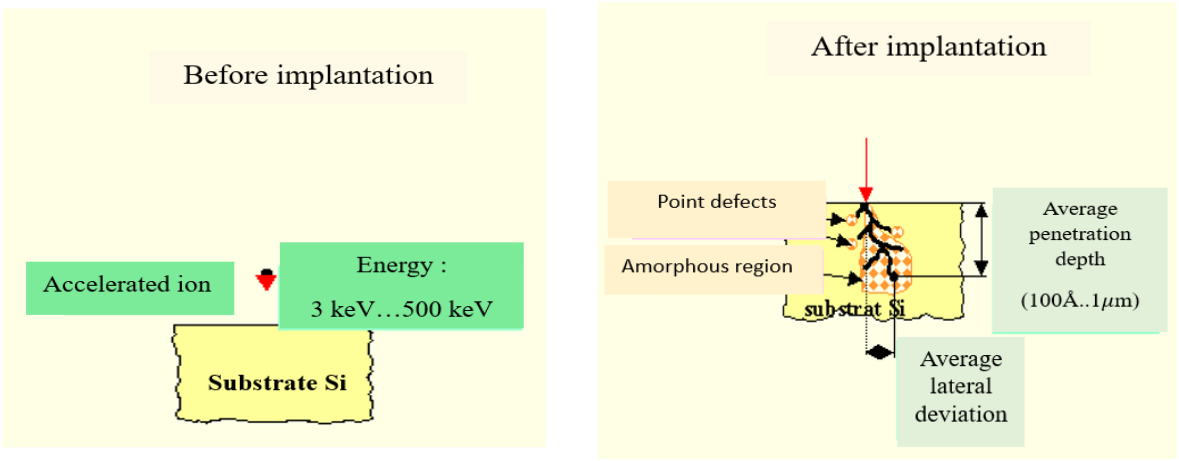



Fig IV.8 Evolution of an ion through the crystal. It creates point defects and amorphises the areas neighbouring its trajectory. Its trajectory is randomly deflected by the atoms in the crystal.

Statistically, the profile obtained is Gaussian in a first approximation.

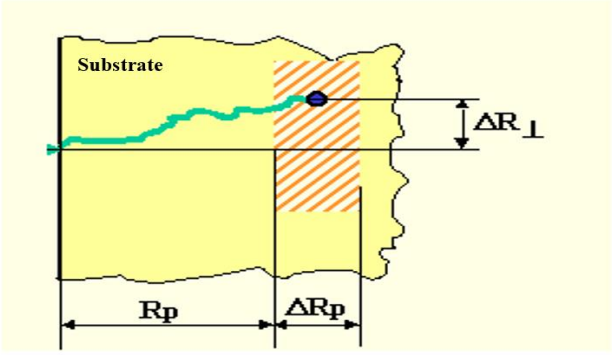



Fig IV.9 Representative ion penetration path into a silicon substrate.

Statistically, the average penetration depth is Rp. Two standard deviations must be considered, one following the direction of incidence, the other perpendicular to it.

$$N(x) = N(R_p)exp\left[-\frac{(x-R_p)^2}{2\Delta {R_p}^2}\right] \quad \text{where} \quad N(R_p) = \frac{\emptyset}{\sqrt{2\pi}\Delta R_p} \approx \frac{0.4\emptyset}{\Delta R_p} \quad \text{(IV.8)}$$

$$\emptyset = \int_0^\infty N(x)\,dx \quad ; \quad \phi \text{ being the implanted dose}$$

In this expression, *N(x)* is the quantity of ions implanted at depth x.

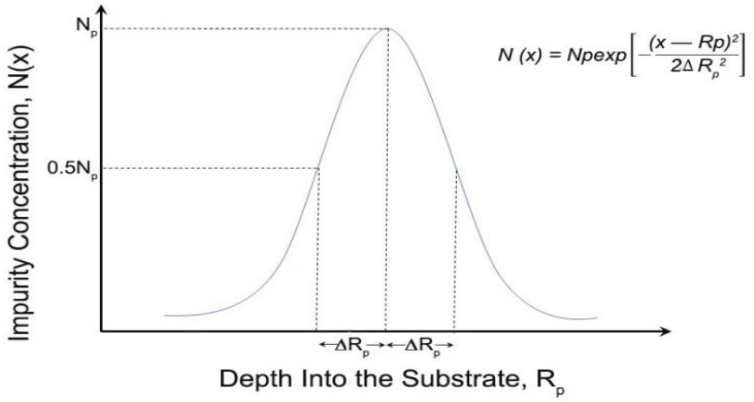



**Fig**. IV.10 Representative dopant profile in a substrate that has undergone ion implantation.

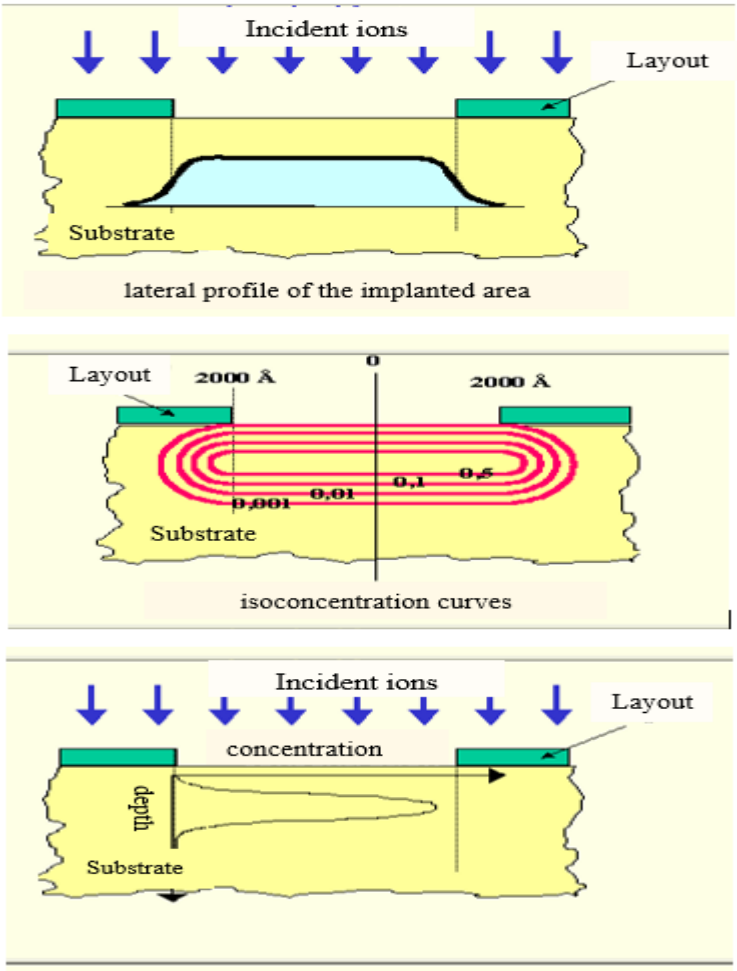
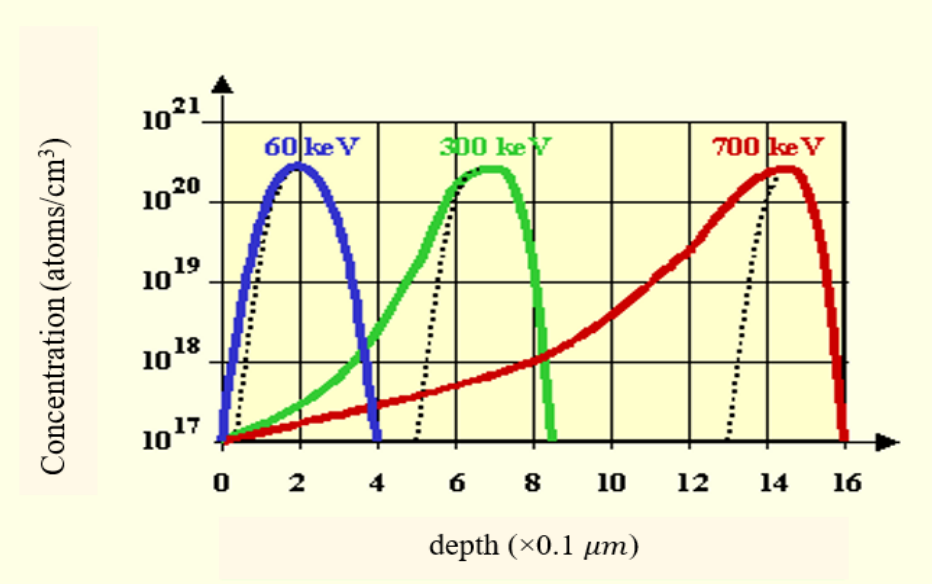



Fig IV.11 Illustration of lateral profiles after implantation through a mask. The isoconcentration curves (relative to the maximum value) are shown in the figure on the right.

Depending on the nature of the implanted ions, more accurate profiles are proposed. For phosphorus or arsenic, 'double Gaussian' models are proposed for which the standard deviation is different before and after the maximum concentration. In the case of boron, for high energies, the profile deviates significantly from the Gaussian. This deviation can be explained simply by the fact that the boron ion, which is very small, can be backscattered in the crystal. In this case, the Pearson-IV profile is used. The figure below shows the profiles obtained following boron implantation at different energies. The deviation from the Gaussian profile is significant before the maxima. This profile can be modelled using the four-momentum method.




IV.12 Distribution of boron atoms implanted in silicon - Pearson-IV profile, 4 moments

**Exercise 1:** Give the correct answer below;( The correct answer is in italics)

1. Ion implantation consists of

a. sending ions created in a plasma to the surface of a substrate located between the plasma electrodes

*b. sending ions accelerated by a strong potential difference to the surface of a substrate*

c. sending atoms into a substrate using an electron beam

d. creating a strong electric field to cause ions brought to the surface of a substrate to penetrate it

2. The average penetration depth of implanted ions depends

a. mainly on the substrate temperature

b. solely on the acceleration energy

*c. on the energy and nature of the implanted ions*

d. on the scanning speed of the implanted ion beam

3. For energies between 10 keV and 500 keV, the penetration depth is between:

*a. 10 nm and 1 µm*

b. 1 nm and 100 nm

c. 10 nm and 100 µm

d. 1 µm and 100 µm

4. The doping profile immediately after implantation can be modelled simply by a function that is:

a. linear

b. exponentially decreasing

c. double exponential

*d. Gaussian*

**Exercise 2:**

The diffusion coefficient $D$ of P-type dopant atoms in oxide ($SiO_2$) has an activation energy $Ea$ = 2.30 eV/atom and a pre-exponential coefficient $D_0 = 5.73 \times 10^{-9}$ m²/s.

Calculate the diffusion length $L = 2\sqrt{Dt}$ in one hour at 1200°C. Given:

$D = D_0 exp\left({-E_a}/{kT}\right)$ with $kT$ (at 1200°C) = 0.127 eV.

**Solution:**

$Ea$ = 2.30 eV/atom, $D_0 = 5.73 \times 10^{-9}$ m²/s

we have , $D = 5.73 \times 10^{-9}\left(\frac{m^2}{s}\right) exp\left({-2.30}/{0.127}\right) = 5.73 \times 10^{-9}\left(\frac{m^2}{s}\right) \times 1.36 \times 10^{-8}$

$$D = 7.8 \times 10^{-17}\left(\frac{m^2}{s}\right)$$

Then, $L = 2\sqrt{Dt}$ , $L = 2\sqrt{7.8 \times 10^{-17}\left(\frac{m^2}{s}\right) \times 3600(s)} = 2 \times 5.3 \times 10^{-7} m$

$$L = 1.06\ \mu m$$

# Chapter V: Oxidation

## V.1 General Concepts

## V.2 Purpose of Oxidation

The oxide layer deposited on silicon has several uses, mainly:

- **Diffusion mask**: (Bipolar and MOS technology) – silicon dioxide prevents the diffusion of substitutional impurities (electrical dopants) into silicon.
- **Dielectric insulating layer**: (MOS technology) – on which a gate metal (Aluminum) is deposited.
- **Protective or passivation layer**: protects the silicon surface against contaminants.

Oxidation is a crucial step in the fabrication of silicon integrated circuits. This specific property of silicon, which is not inherently a very good semiconductor, has made it the most widely used material in microelectronics. Producing a high-quality oxide is essential throughout modern IC manufacturing processes.

Silicon dioxide ($SiO_2$) acts as a barrier against diffusion or ion implantation, preventing impurities from entering regions where conductivity type must remain unchanged. This is possible because the diffusion coefficient of impurities in $SiO_2$ is much lower than in silicon.

Table V.1. Diffusion Coefficients of Dopants in $SiO_2$ and Si

| Dopant Element | D ($cm^2/s$) in $SiO_2$ (oxide) | D ($cm^2/s$) in Silicon |
|---|---|---|
| Boron (B) | $\approx 1\times10^{-15}$ | $\approx 3\times10^{-13}$ |
| Phosphorus (P) | $\approx 1\times10^{-14}$ | $\approx 3\times10^{-12}$ |
| Arsenic (As) | $5\times10^{-15}$ | $\approx 5\times10^{-14}$ |
| Antimony (Sb) | $9\times10^{-17}$ | $\approx 2.5\times10^{-14}$ |

### Thin Oxide Layers for MOS Transistors

The silicon dioxide layer forming the gate of MOS transistors (20–500 Å thick) requires special precautions. It is generally obtained by **thermal oxidation**, a method that ensures the lowest density of interface traps at the $Si/SiO_2$ boundary.

**Importance of Silicon Oxidation**

Oxidation is a very important step in the manufacture of silicon integrated circuits, since it is thanks to this specific property that silicon, which is not a very good semiconductor in itself, has become the most widely used material in microelectronics. This operation is necessary throughout modern integrated circuit manufacturing processes. It is therefore essential to know how to produce a good quality oxide.

## 2.1 Different Types of Oxidations

It should be noted that we will differentiate between the technological oxidation process and the oxide deposition process, which does not involve the same constraints, particularly thermal ones. The oxidation process therefore consists of oxidising the silicon from the surface of the substrate. The main reactions are as follows:

The oxide layer can be obtained either by:

**Direct Thermal Oxidation**

Depending on the oxidizing agent, we distinguish:

**2.1.1 Dry Oxidation (DRY)** Performed in a flow of dry oxygen gas:

$$Si(s) + O_2 \rightarrow SiO_2(s)$$

Dry Oxidation: A Precise Process

In dry oxidation, wafers are heated to 1000–1200 °C (about 2000 °F) in an oxidation furnace and exposed to pure oxygen ($O_2$). High-quality oxide with few vacancy defects is produced when the oxide grows slowly according to the formula $Si + O_2 \rightarrow SiO_2$. This particular method is frequently applied to dielectrics in capacitors and extremely thin gate oxides (GOX) in field-effect transistors.

**2.1.2 Wet Oxidation (WET or STEAM)** Much faster, oxygen is enriched with water vapor:

$$Si(s) + 2H_2O \rightarrow SiO_2(s) + 2H_2(g)$$

The wafer is first exposed to steam during the wet oxidation process when oxygen passes via boiling water. At temperatures between 950 and 1000 °C (about 1800 °F), the reaction proceeds according to the formula $Si + 2H_2O \rightarrow SiO_2 + 2H_2$. Wet oxidation happens far more quickly than dry oxidation. However, it yields a lower-quality oxide and is more difficult to manage. Because of this, moist oxidation is used more frequently to produce field oxide (FOX). The field oxide, which serves to laterally isolate areas from one another, is the first thick oxide layer that is directly formed on silicon. Field oxide was only generated in silicon regions devoid of devices in previous

techniques. The term "field oxide" comes from the fact that these areas were called "non-active" or "field" regions.

**Note:** These reactions occur very quickly at high temperature, forming a so-called **native oxide** (15–30 Å).

- **Oxide Deposition**

Oxide layers can also be deposited by:

- Atmospheric Pressure Chemical Vapor Deposition (CVD)
- Low Pressure CVD (LPCVD)
- Plasma-assisted CVD

- **Quality Considerations**

For electronic-grade oxide, **thermal oxidation** is preferred:

- Oxidation with pure $O_2$ → slower growth, better electronic properties (fewer electrically active defects).
- Oxidation with $H_2O$ vapor → faster growth, but more electrical defects. → This method is preferred for **thick oxides** (≈1000 Å) used for masking or isolation.

- **Native Oxide and Passivation**

Silicon oxidizes at room temperature in air (due to oxygen).

- Once the oxide reaches 2–3 atomic layers, oxidation stops.
- This thin layer is called a **passivating oxide**.

- **Advantages of CVD Oxides**

Silicon dioxide layers deposited by CVD:

- Provide faster growth rates than thermal oxidation.
- Used to isolate multiple devices from each other.
- Serve as a barrier during ion implantation.
- Increase the thickness of a thermally grown oxide layer.

**1. Principle of Thermal Oxidation**

Thermal oxidation is carried out in a heated furnace where silicon wafers, held upright in a quartz tube, are exposed to temperatures between **900 and 1200°C**.

- An oxidizing gas is introduced into the furnace:
  - **Dry oxidation** → oxygen gas ($O_2$)
  - **Wet oxidation** → water vapor ($H_2O$)

The installation must be carefully controlled:

- Gas flow regulation
- Automatic wafer loading
- Degassing
- Temperature control within ±1°C

These precautions are necessary to avoid thermal shocks to the wafers.

**2. Silicon Layer Consumed During Oxide Growth**

Oxidation does not occur at the surface of the oxide layer but at the **$SiO_2$/Si interface**.

- Oxidizing species ($O_2$, $H_2O$) must diffuse through the existing oxide layer.
- Verified experimentally using radioactive tracers.

The initial silicon layer reacts with the oxidising agent to form $SiO_2$; This consumes silicon. The $Si/SiO_2$ interface will therefore end up 'below' the initial surface. A simple calculation shows that the fraction of thickness located 'below' the initial surface represents 46% of the total thickness of the oxide; the fraction 'above' therefore represents 54% (figure).

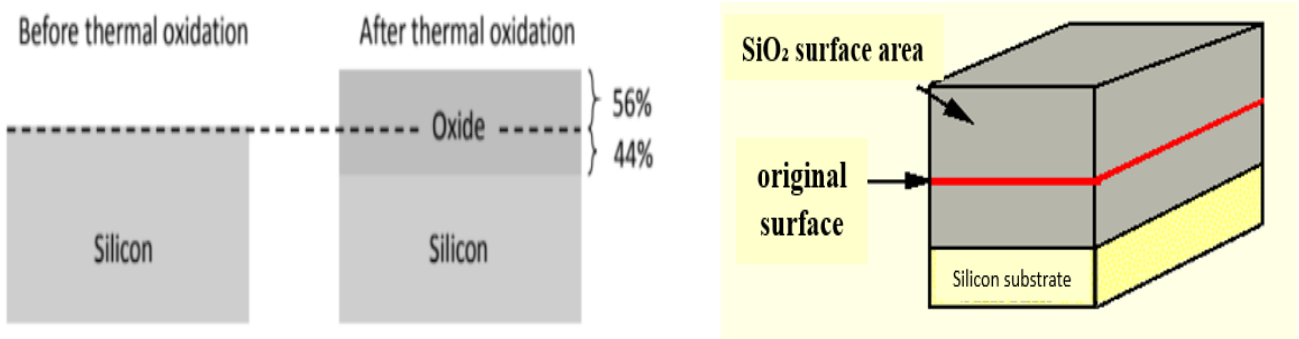



Fig. V.1 Silicon oxidation. Part of the substrate was consumed during oxidation.

This increase in volume will have significant consequences on the flatness of the wafer surface when localized oxidation is carried out. Indeed, the increase in volume will be localised and will therefore create a relief as shown in the figure.

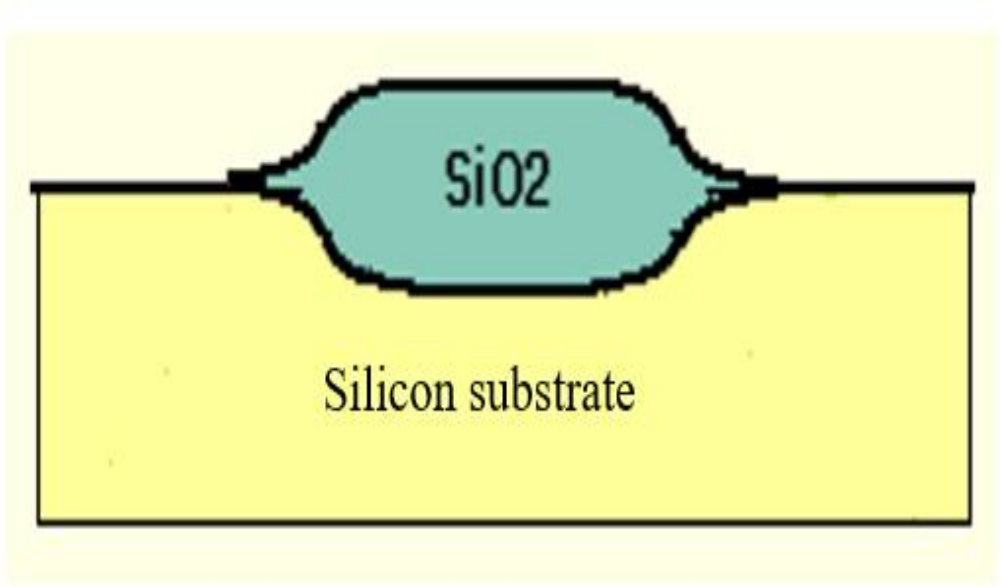



Fig V.2 Effect of localised oxidation of silicon. The increase in volume creates a relief pattern. on the surface of the wafer.

**Consequence:** During oxide growth, a portion of silicon is consumed.

Constants :

- $N_{ox} = 2.3 \times 10^{22}\ cm^{-3}$
- $N_s = 5.0 \times 10^{22}\ cm^{-3}$

Formula:

$$X_s = \frac{N_{ox} \cdot X_{ox}}{N_s} \Rightarrow X_s = 0.46\, X_{ox} \qquad \text{(V.1)}$$

Thus, for an oxide thickness $X_{ox}$, a silicon thickness of $X_S$ = **0.46** $X_{ox}$ is consumed.

**Diagram Explanation**

- Growth of $SiO_2$ consumes part of the silicon wafer.
- Because one mole of $SiO_2$ occupies more volume than one mole of Si, the oxide layer expansion results in a reduction of the underlying silicon thickness.

Oxidation processes are generally carried out in furnaces in which dry or moist oxygen or steam is circulated (see Fig V.3): However, in submicron technologies, wafers can be treated in reactors heated very rapidly by lamps (halogen type) in the presence of an oxidizing agent. This technique is called rapid thermal oxidation.

Water vapor can also be created in the furnace by synthesizing it from a hydrogen flow and an oxygen flow. This reaction is highly exothermic and therefore dangerous. The device therefore contains a large number of safety features (flame detection, flow control, etc.) to prevent any explosion.

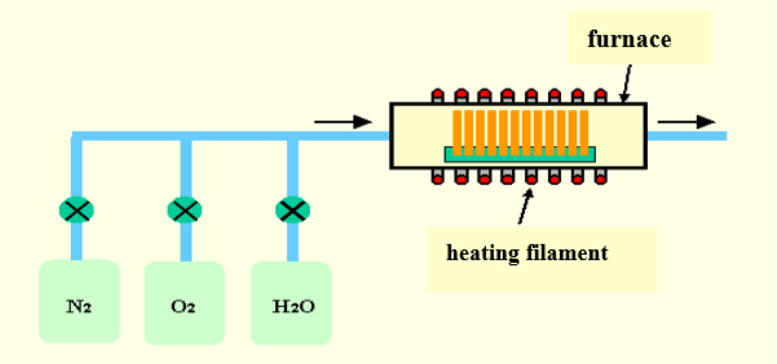


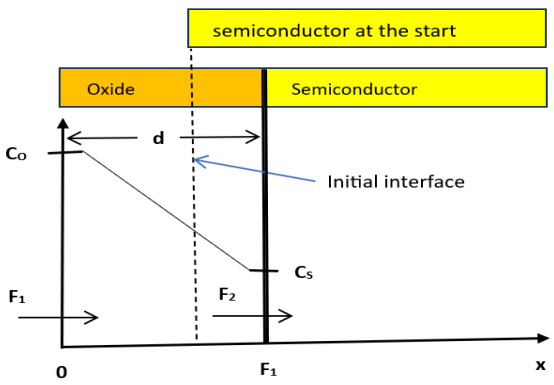

Fig V.3 Thermal oxidation with oxygen or steam.

## 3. Kinetics of Oxide Growth

### 3.1 Deal–Grove Model (Oxidation Modeling)

The Deal–Grove model assumes:

- Pressure = 1 atm
- Oxide thickness between 0.03 and 2 µm
- Temperature between 700 and 1300°C



### 3.2 Distinct Regions in Oxidation

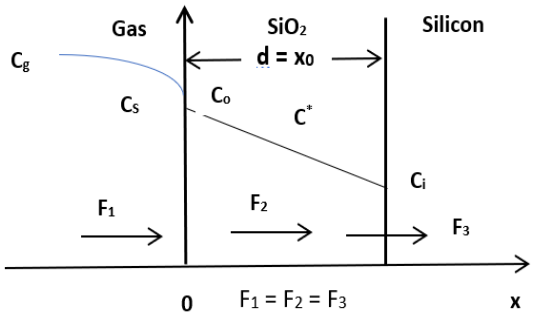
Oxidation involves three regions:

1. **Gas flow** – located in the diffusion tube.
2. **Oxide layer ($SiO_2$)** – formed at the silicon surface.
3. **Silicon wafer (Si)** – the substrate being oxidized.

### 3.3 Flux Determination

The calculation is based on the flux of oxidizing species across these regions.

In steady-state conditions :




Basic model for thermal oxidation

$$F_1 = F_2 = F_3 \qquad \text{(V.1)}$$

where:

- $F_1$= flux in the gas phase
- $F_2$= flux through the oxide layer
- $F_3$= flux at the silicon interface

Thus, the oxidation process is modeled by equating these fluxes, forming the basis of the **Deal–Grove thermal oxidation model**.

### 3.4 Flux Modeling in Oxidation

#### Oxidizing Species Fluxes

- **Flux $F_1$**: Oxidizing species diffuse in the gas phase up to the gas/solid interface.
- **Flux $F_2$**: Oxidizing species diffuse in the solid phase through the oxide layer toward the $SiO_2$/Si interface.
- **Flux $F_3$**: Oxidizing species react at the silicon surface.

**Concentration Definitions**

- $C_g$: Concentration of oxidizing species in the gas (atmosphere)
- $C_s$: Concentration at the oxide surface
- $C_o$: Concentration in the oxide
- $C_i$: Concentration at the $SiO_2$/Si interface

**Flux $F_1$ Expression**

Flux $F_1$ is governed by mass transfer in the gas phase and estimated by:

$$F_1 = h_g(C_g - C_s) \quad \text{(V.2)}$$

where:

- $h_g$: Mass transfer coefficient in the gas phase

Using the ideal gas law, concentrations $C_g$ and $C_s$ relate to partial pressures:

$$C = \frac{P}{kT} \quad \text{(V.3)}$$

Thus: $C_g = \frac{P_g}{kT}$ away from the surface

$C_s = \frac{P_s}{kT}$ close to the surface

**Expressing $F_1$ in Terms of Solid Concentrations**

To express $F_1$ using $C_o$(oxide interface) and $C^*$(initial oxide concentration), we apply **Henry's Law**:

- At equilibrium, the concentration of a species in a solid is proportional to its partial pressure in the surrounding gas.

  For: $C_o$ : the environment is $P_s$

  $C^*$ : the environment is $P_g$

$$C_o = HP_s \quad , C^* = HP_g \quad \text{(V.4)}$$

where $H$ is Henry's constant.

Substituting into the flux equation:

$$F_1 = h_g\left(\frac{P_g}{kT} - \frac{P_s}{kT}\right) = \frac{h_g}{kT}(P_g - P_s) = \frac{Hh_g}{HkT}(P_g - P_s) \quad \text{(V.5)}$$

Using Henry's law:

$$F_1 = \frac{h_g}{HkT}\left(HP_g - HP_s\right) = \frac{h_g}{HkT}(C^* - C_o) \quad \text{(V.6)}$$

$$\longrightarrow \quad F_1 = h(C^* - C_o) \quad \text{(V.7)}$$

where: $h = \frac{h_g}{HRT} \longrightarrow$ mass transfer coefficient from gas to solid

Final expression:

$$F_1 = h(C^* - C_o) \quad \text{(V.8)}$$

### 3.5 Flux Equations and Concentration Profiles

#### Flux $F_2$ – Diffusion Through the Oxide

The oxidizing species diffuse through the oxide layer according to **Fick's First Law**:

$$F_2 = D \cdot \frac{(C_o - C_i)}{x_o} \quad \text{(V.9)}$$

or equivalently:

$$F_2 = -D \cdot \frac{(C_i - C_o)}{x_o} \quad \text{(V.10)}$$

where :

- $x_o$: oxide thickness ($SiO_2$)
- $D$: diffusion coefficient of the oxidizing species in $SiO_2$

#### Flux $F_3$ – Chemical Reaction at the $SiO_2$/Si Interface

The flux of chemical reaction at the interface is proportional to the concentration of the oxidizing species at the $SiO_2$/Si boundary:

$$F_3 = k_s C_i \quad \text{(V.11)}$$

where:

$k_s$: chemical reaction rate constant at the $SiO_2$/Si interface

#### Equilibrium Condition

At equilibrium:

$$F_1 = F_2 = F_3 = F \quad \text{(V.12)}$$

The flux value is expressed as:

$$F = \frac{k_s \cdot C^*}{1 + \frac{k_s}{h} + \frac{k_s \cdot x_o}{D}} \quad \text{(V.13)}$$

where $F$ is equilibrium flux value as a function of concentration in $SiO_2$

**Concentrations at Interfaces**

Let's determine the concentrations $C_o$ and $C_i$ as a function of $C^*$

Either:

$$h(C^* - C_o) = D \cdot \frac{(C_o - C_i)}{x_o} = k_s C_i = \frac{k_s \cdot C^*}{1 + \frac{k_s}{h} + \frac{k_s \cdot x_o}{D}} \quad \text{(V.14)}$$

- **Gas/Oxide Interface**:

$$C_o = \left( \frac{1 + \frac{k_s \cdot x_o}{D}}{1 + \frac{k_s}{h} + \frac{k_s \cdot x_o}{D}} \right) \cdot C^* \quad \text{(V.15)}$$

- **$SiO_2$/Si Interface**:

$$C_i = \frac{C^*}{1 + \frac{k_s}{h} + \frac{k_s \cdot x_o}{D}} \quad \text{(V.16)}$$

where:

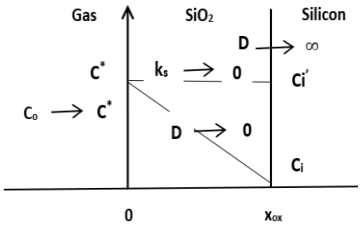
- $C^*$: concentration of oxidizing species in the oxide at equilibrium
- $h$: mass transfer coefficient in the gas phase

**3.6 Limiting Cases in Oxidation**

Two limiting cases are frequently encountered in this type of process:

**(i) Very low diffusion coefficient (D → 0):**

- Then $C_i \to 0$and $C_o \to C^*$.
- The reaction is said to be **diffusion-limited** (very low $C_i$→ insufficient supply of oxidizing species).




**(ii) Very high diffusion coefficient (D → ∞):**

- Then $C^* \to C_o$.
- When the reaction constant $k_s \ll h$, we have $C_i \approx C_o \approx C^*$.
- The consumption of species at the $SiO_2$/Si interface is weak, and there is no concentration gradient in the oxide.
- The oxidation reaction is **reaction-rate limited**.

### 3.7 Oxide Growth Rate

The oxide layer grows at a rate:

$$v = \frac{dx_{ox}}{dt} \tag{V.17}$$

The flux of oxidizing species can be expressed in terms of the number $N$ of oxidizing molecules per unit volume:

$$F = Nv = J = nqv \quad ; \text{ current density} \tag{V.18}$$

$$\begin{cases} F: \text{flux} \\ N: nb\,.molecules \\ v: rate \end{cases}$$

Or:

$$F = k_s \cdot C_i = \frac{N dx_{ox}}{dt} \tag{V.19}$$

Thus: the oxide growth rate as :

$$\frac{dx_{ox}}{dt} = \frac{k_s \cdot C_i}{N} = \frac{k_s \cdot C^*}{N\left(1 + \frac{k_s}{h} + \frac{k_s \cdot x_{ox}}{D}\right)} \tag{V.20}$$

Where:

- $N = 2.9 \times 10^{22}$molecules of $SiO_2/cm^3$

### 3.8 Kinetic Law of Oxide Growth

To determine the variation law $x_{ox} = f(t)$, we integrate the previous equation with the initial condition:

$$x_{ox}(t = 0) = x_1$$

Where $x_1$represents the initial oxide thickness due to:

- A previous oxidation, or
- The native oxide present on any Si wafer exposed to air.

Thus: $x_{ox}(t) = x$

$$N\left(1 + \frac{k_s}{h} + \frac{k_s \cdot x_{ox}}{D}\right) dx_{ox} = k_s \cdot C^* \cdot dt \tag{V.21}$$

### 3.9 General Oxidation Equation

By integrating the flux equations, we obtain:

Integration gives:

$$\int_{x_1}^{x_{ox}} N\frac{k_s x_{ox}}{D}dx_{ox} + \int_{x_1}^{x_{ox}} N\left(1+\frac{k_s}{h}\right)d\,x_{ox} = \int_0^t k_s \cdot C^* \cdot dt$$

$$\int_{x_1}^{x_{ox}} \frac{N}{DC^*}x_{ox}dx_{ox} + \int_{x_1}^{x_{ox}} \frac{N}{C^*}\left(\frac{1}{k_s}+\frac{1}{h}\right)d\,x_{ox} = \int_0^t dt$$

$$\frac{N}{2DC^*}({x_{ox}}^2 - {x_1}^2) + \frac{N}{C^*}\left(\frac{1}{k_s}+\frac{1}{h}\right)(x_{ox}-x_1) = t$$

$$\frac{{x_{ox}}^2}{B} + \frac{Ax_{ox}}{B} = t + \frac{{x_1}^2 + Ax_1}{B} \qquad \text{(V.22)}$$

By posing : $\begin{cases} A = 2D\left(\frac{1}{k_s}+\frac{1}{h}\right) \\ B = \frac{2DC^*}{N} \end{cases}$

the solution to the quadratic equation: $${x_{ox}}^2 + Ax_{ox} = B(t+\tau) \qquad \text{(V.23)}$$

This is the **general equation governing silicon oxidation**.

$$\frac{{x_{ox}}^2}{B} + \frac{x_{ox}}{({}^B/_A)} = t + (t+\tau) \qquad \text{(V.24)}$$

With: $\tau = \frac{{x_1}^2 + Ax_1}{B}$ ; is written:

### 3.10 Solution of the Quadratic Equation

The solution can be expressed as:

$$x_{ox} = \frac{A}{2}\left\{\sqrt{1+\frac{(t+\tau)}{{A^2}/{4B}}} - 1\right\} \qquad \text{(V.25)}$$

This relation describes the variation of oxide thickness $X_{ox}$as a function of time $t$.

### 3.11 Experimental Behavior

Figure 3 illustrates the variation of $\frac{x_{ox}}{A/2}$ with $\frac{(t+\tau)}{{A^2}/{4B}}$. Experimental points correspond to different conditions (temperature, dry or wet atmosphere).

Two regimes are observed:

- **Diffusion-controlled growth** (low diffusion coefficient $D$)
- **Reaction-controlled growth** (high diffusion coefficient $D$)

This Fig V.4 compares experimental oxidation data at different temperatures with theoretical models. The dimensionless plot highlights two regimes: reaction-controlled growth at short times and diffusion-controlled growth at long times. The alignment of data points with the theoretical curves confirms the validity of the general oxidation equation.

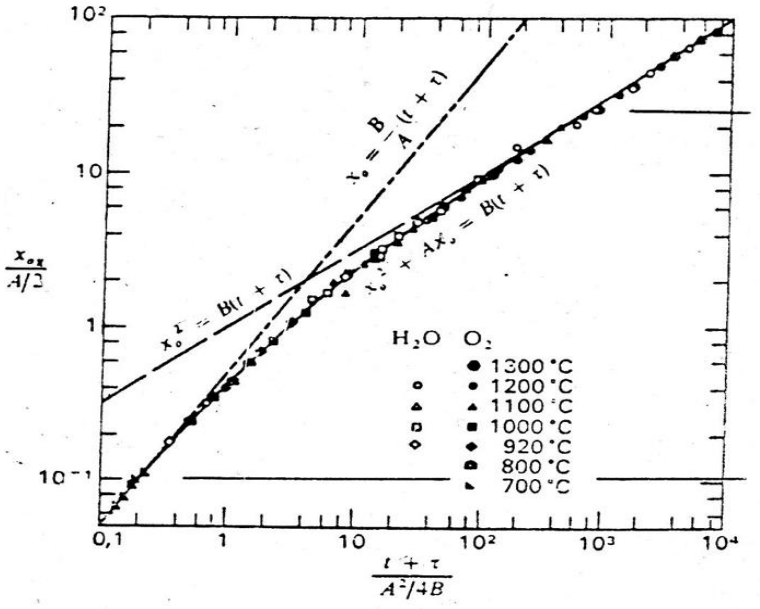



Fig. V.4 Oxidation of Si and general relationship between its two forms

### 3.12 Limiting Case – Linear Growth (Compare *A* and *B/A*)

For short times ($t + \tau \ll A^2/4B$):

- Neglecting $x_{ox}^2$compared to $x_{ox}$, the equation simplifies to:

$$x_{ox} = \frac{B}{A}(t + \tau)$$

This corresponds to the **linear growth regime**, where oxidation is controlled by the **surface reaction rate**.

This figure. 17 shows the linear rate constant (*B/A*) plotted against (*1/T)* for wet and dry oxidation. The slope of each curve provides the activation energy, highlighting differences between the two ambients. The results confirm that oxidation kinetics are strongly dependent on temperature and atmosphere.

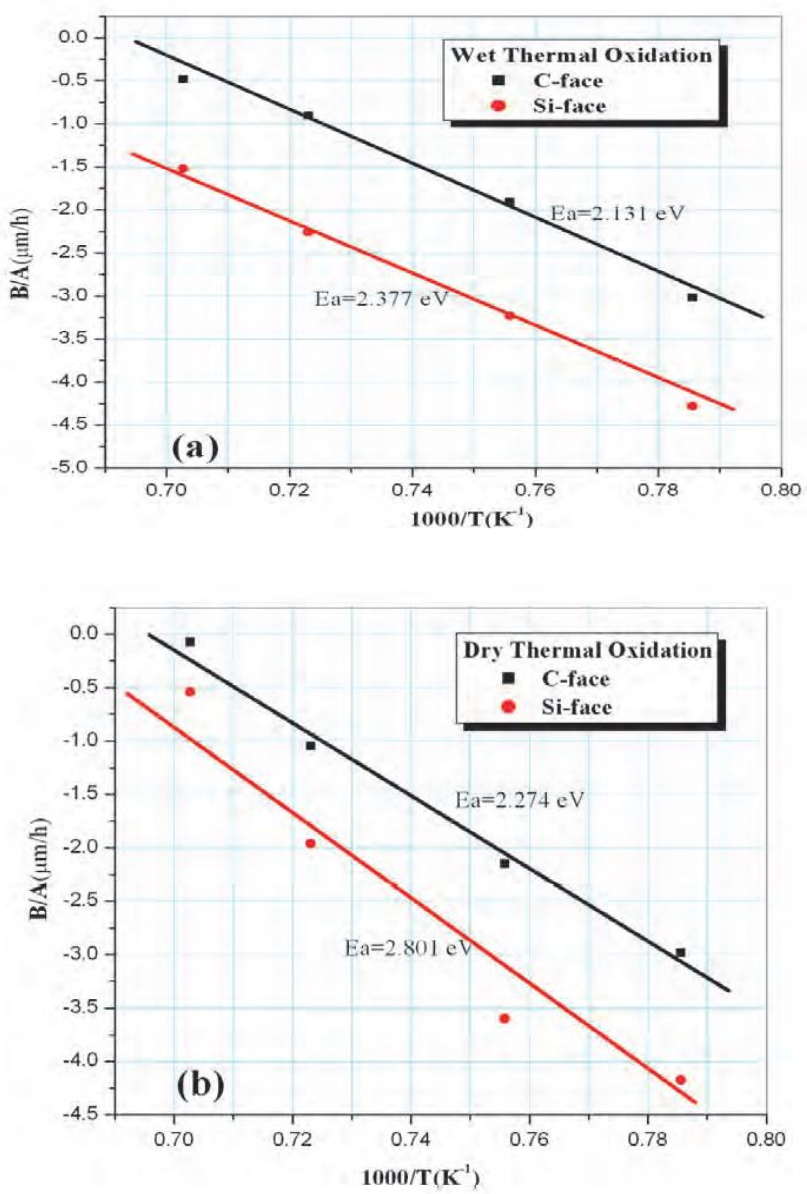



Fig. V.5 (a) Linear rate constant (B/A) as a function of 1/T for oxidation in wet ambient and (b) in dry ambient. Calculated activation energy is shown in their respective plots

### 3.13 Oxidation Regimes

#### (i) Linear Growth Regime – Reaction-Controlled

For short diffusion times and thin oxide layers, oxidizing species diffuse easily through $SiO_2$ to the $SiO_2$/Si interface.

- Diffusion is much faster than the oxidation reaction with silicon.
- The oxidation process is **limited by the reaction rate**.

Growth rate expression:

$$\frac{B}{A} = \frac{k_s h C^*}{(k_s + h) \cdot N} \qquad \text{(V.26)}$$

→ This corresponds to the **linear regime**.

**(ii) Parabolic Growth Regime – Diffusion-Controlled**

For long times $t \gg \frac{A^2}{4B}$:

- $h$and $k$are much greater than $D$
- $A$ becomes small and $B$large
- Neglecting $A/B$ compared to $\frac{x_{ox}^2}{B}$ in the general equation

Resulting in:

$$x_{ox} = \sqrt{B(t+\tau)} \qquad \text{(V.27)}$$

For long times $t \gg \tau$:

$$x_{ox} = \sqrt{Bt}$$

→ Oxidation is **controlled by diffusion** (low $D$) → $B = \frac{2DC^*}{N}$is called the **parabolic constant**

In this regime, thick oxide layers form.

- The oxidation reaction at the $SiO_2$/Si interface depends on the time required for oxidizing species to diffuse through the oxide layer.
- The process is **diffusion-limited**.

**4. Thermal Oxidation Equipment**

Silicon wafers are placed on a fused silica ($SiO_2$) comb and introduced into the center of an open tube.

- The tube is swept by an oxidizing gas flow ($O_2$, $H_2O$ with $N_2$, HCl).
- The central part of the tube is inside a high-temperature furnace (800–1200°C).
- The furnace has three independently powered heating coils.
- These coils create a **flat temperature profile** over ≈50 cm with ±0.1°C precision.

In industry:

- Wafer loading and unloading is automated with programmable speed.
- The furnace is continuously heated to ≈800°C and flushed with a neutral gas (Ar, $N_2$).

### 5. Oxidizing Gases and Flow Control

Ultra-pure oxidizing gases, with flow rates controlled by a monitoring system, pass through glass conduits into the oxidation tube.

- The gas stream always enters from the **back side of the wafers**.

**Types of Oxidizing Atmospheres**

- **Dry $O_2$**: Pure oxygen gas directly introduced into the oxidation tube.
- **Wet Oxidation (WET or STEAM)**:
  - **By bubbling**: The oldest technique, where dry oxygen is bubbled through deionized water heated to 95°C → humid oxygen (wet $O_2$).
  - **By hydrogen–oxygen combustion**: At the furnace entrance, known as the "torch" method → steam atmosphere. Requires safety measures due to $H_2$ use.
  - **By direct vapor injection**: Deionized water heated to 100°C produces steam, which mixes with the dry $O_2$ flow.

### 6. Advantages of Thermal Oxidation

- The silica ($SiO_2$) obtained is perfectly **amorphous**.
- The **$SiO_2$/Si interface quality** is reproducible for a given crystalline orientation of the substrate.
- The process is **collective**: up to 200 wafers can be treated simultaneously.
- The oxide layers are highly **homogeneous** (both thin layers ≈100 Å and thick layers ≈1.5 µm).
- The process is easily **automated** (loading/unloading systems, programmed sequences, temperature cycles, etc.).

### 7. Alternative Oxidation Methods

In some cases, it is impractical or impossible to grow a $SiO_2$ film by thermal oxidation—for example, when a masking oxide must be grown on **$Si_3N_4$** already deposited on silicon.

In such cases, the oxide is deposited by one of the following methods:

- **Chemical Vapor Deposition (CVD)** of silica
- **Anodic oxidation**
- **Plasma oxidation** in oxygen

⚠ Note: Oxides obtained by these methods are of **lower quality** compared to thermal oxidation.

## 8. Alternative Oxidation Processes

### 8.1 Chemical Vapor Deposition (CVD) of $SiO_2$

**Principle:** A gaseous compound is introduced into a chamber, decomposing under heat. One of the decomposition products is solid (here: $SiO_2$).

**Most common reaction:** Pyrolysis of silane in the presence of oxygen:

$$SiH_4(g) + 2O_2 \overset{100-200^\circ C}{\rightarrow} SiO_2(s) + 2H_2O$$

- Growth rates: several hundred Å/min → ≈10 times faster than thermal oxidation.
- Mixing silane with **$B_2H_6$** or **$PH_3$** produces **boron- or phosphorus-doped $SiO_2$ layers**.
- Doped oxide can serve as a **dopant source for diffusion**.
- Films are not always effective as protective layers due to low density. → Density can be increased by annealing at **800–900°C for 15 min** in the presence of water vapor.

### 8.2 Anodic Oxidation

**Principle:** Electrolytic oxidation in a bath.

**Electrolytic bath composition:**

- Ethylene glycol
- $KNO_3 + H_2O$

**Reactions:**

$$Si + 2H_2O \rightarrow SiO_2 + 4H^+ + 4e^-$$
$$4e^- + 4H_2O \rightarrow 2H_2 + 4OH^-$$

- Consumes a thin layer of silicon.
- Simple to perform at room temperature.
- Produces oxides of **poor electrical quality**.

### 8.3 Plasma Oxidation (Reactive Sputtering)

**Principle:**

- Electrical discharge in a gas → cathode disintegration under ion bombardment.
- Cathode particles are transported by kinetic energy or diffusion.
- Extracted silicon is oxidized in the plasma gas.

**Conditions:**

- Reactive gas: Argon mixed with $O_2$ (plasma).
- Cathode voltage: –3 kV.
- Pressure: 0.02–0.2 torr.
- Growth rate: ≈100 Å/min.

**Advantages:**

- Fast growth
- Low temperature process

**Limitations:**

- Produces oxides of **relatively low quality**.

**Exercise :**

The expression $x_{ox}$ for the oxide layer on the surface of thermally oxidized silicon is given by the expression:

$$x_{ox} = \left[\left(1 + \frac{t+\tau}{A^2/4B}\right)^{1/2} - 1\right]\frac{A}{2}$$

At 1200°C, the linear and quadratic growth rate constants are given in the table below:

Determine the oxidation time required to grow a 0.1 μm layer of $SiO_2$ for:

a- Dry oxidation. Write the corresponding chemical reaction.

b- Wet oxidation. Write the corresponding chemical reaction.

c- Conclusion (compare a- and b-).

| | Oxidation coefficents for silicon | | | | | |
|---|---|---|---|---|---|---|
| | Dry (sèche) | | | | Wet (humide) | |
| Temperature (°C) | A (μm) | B (μm²/hr) | τ (hr) | | A (μm) | B (μm²/hr) |
| 800 | 0.370 | 0.0011 | 9 | | / | / |
| 920 | 0.235 | 0.0049 | 1.4 | | 0.50 | 0.203 |
| 1000 | 0.165 | 0.0117 | 0.37 | | 0.226 | 0.287 |
| 1100 | 0.090 | 0.027 | 0.076 | | 0.11 | 0.510 |
| 1200 | 0.040 | 0.045 | 0.027 | | 0.05 | 0.720 |

**Solution :**

Let us express *t* in terms of $x_{o_x}$; we find:

Then : $t = \frac{A^2}{4B}\left[\left(1+\frac{2x_{ox}}{A}\right)^2 - 1\right] - \tau$ $x_{ox}$ =0.1 $\mu m$

c- Let us determine *t* for wet oxidation.:

T= 1200°C, A = 0.05 $\mu m$, B = 0.720 $\mu m^2/hr$ and $\tau = 0$

$t = \frac{(0.05)^2(\mu m^2)}{4\times 0.720(\mu m^2/hr)}\left[\left(1+\frac{2\times 0.1(\mu m)}{0.05(\mu m)}\right)^2 - 1\right] - 0 = 0.020\ hr$

$t = -0.020\ hr$ or 1.2 *mn*

Corresponding chemical reaction:

$$Si(s) + 2H_2O \rightarrow SiO_2(s) + 2H_2(g)$$

d- Let us determine *t* for dry oxidation:

T= 1200°C, A = 0.040 $\mu m$, B = 0.045 $\mu m^2/hr$ and $\tau = 0.027\ hr$

$t = \frac{(0.040)^2(\mu m^2)}{4\times 0.045(\mu m^2/hr)}\left[\left(1+\frac{2\times 0.1(\mu m)}{0.040(\mu m)}\right)^2 - 1\right] - 0.027 = 0.283\ hr$

$t = -0.283\ hr$ or 17 *mn*

Corresponding chemical reaction:

$$Si(s) + O_2 \rightarrow SiO_2(s)$$

e- Conclusion : Dry oxidation is slower than wet oxidation, but it produces fewer defects.

# Chapter VI : Photolithography

## VI.1 Definition:

The process of transferring a mask (physical or software) to the wafer is called **photolithography**. This word is derived from lithos (Greek for stone) and photography. Photolithography is the process of etching a thin layer of a given material according to a specific pattern. The pattern to be etched is initially (in positive or negative) on a medium called a mask. This is a glass plate with a layer of chrome or gelatine on which the pattern to be reproduced has been etched.

This is a photographic process that allows the etching of one or more solid layers, such as nitrides, oxides, metals, etc., according to a well-defined pattern. The light used is generally outside the visible spectrum, namely in the ultraviolet or even X-ray range.
The manufacturing of the masks and the steps that lead to the transfer of the design constitute **microlithography** (which is the reproduction of designs on the micron scale).

## VI.2 Principle of photolithography:

Figures a and b recall the principle of the photolithography process; the objective is to transfer a pattern (for example a rectangle which will correspond to a source area) made on a mask to a layer of the plate.

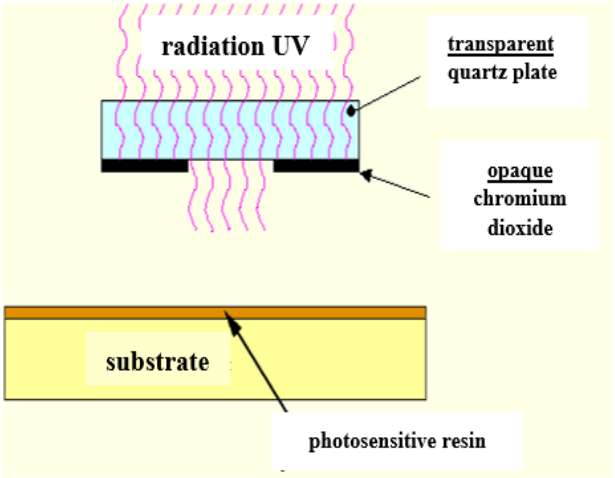



Fig VI.1 a: photolithography mask. The use of quartz is linked to the nature of photons, which are generally in the ultraviolet range. Chromium dioxide is opaque to this radiation and allows for good definition of the basic patterns.

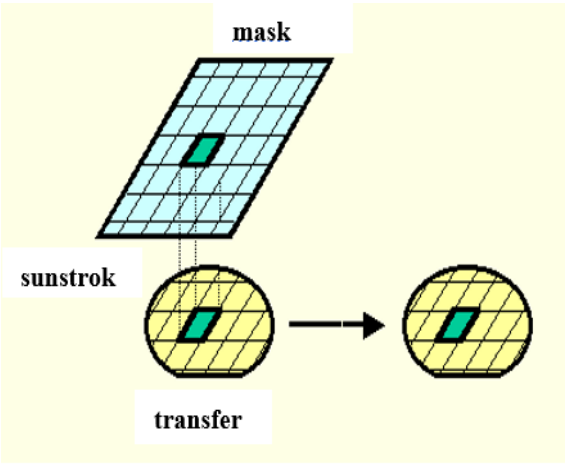
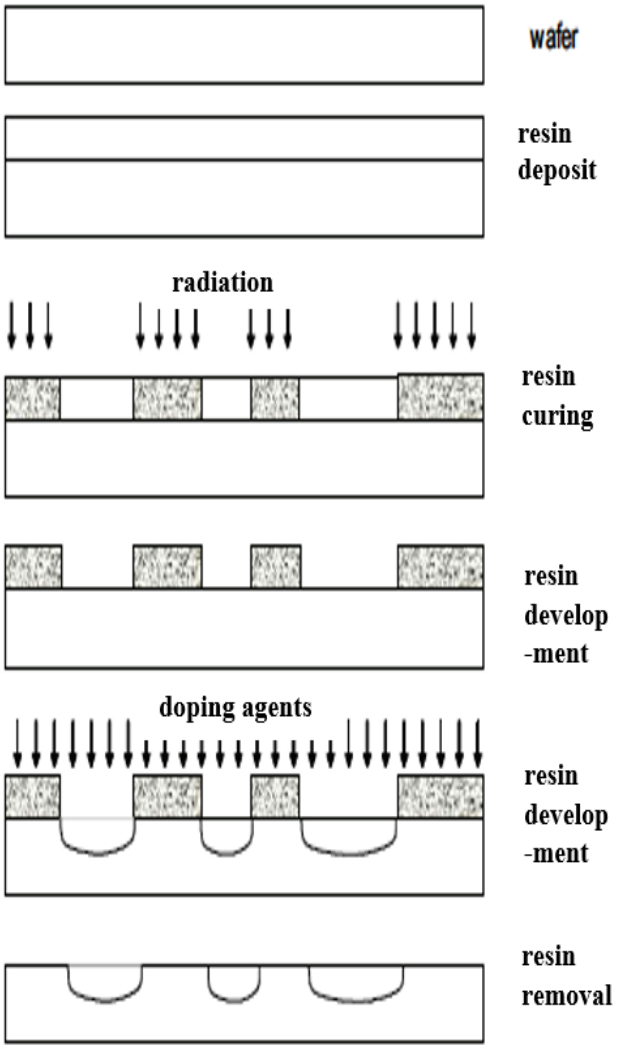



Figure b: principle of photolithography: through exposure to light, the pattern defined on the mask is transferred to the wafer.

Let us imagine the simple case of manufacturing an n-doped area on a p-doped wafer. In the first phase, a resin is deposited on the wafer. In the second phase, radiation is sent onto the resin with spatial modulation representing the pattern to be created. In industrial processes, radiation is generally light, mainly ultraviolet. The exposed areas of the resin undergo a change in their chemical properties. For example, they will be more resistant to the action of solvents. The fourth step is the dissolution of the unexposed areas of the resin. The reverse is also possible, in which case the exposed areas are dissolved more easily. In a fifth step, the ions to be included to dope the silicon (phosphorus for n-type doping) are diffused into the areas not covered by resin. Finally, in the sixth step, the resin is removed to obtain the required structured wafer. The shaded areas are doped n and can, for example, form the wells of PMOS transistors.




The photolithography process takes place in the following sequence: (Example: P-N junction diodes).

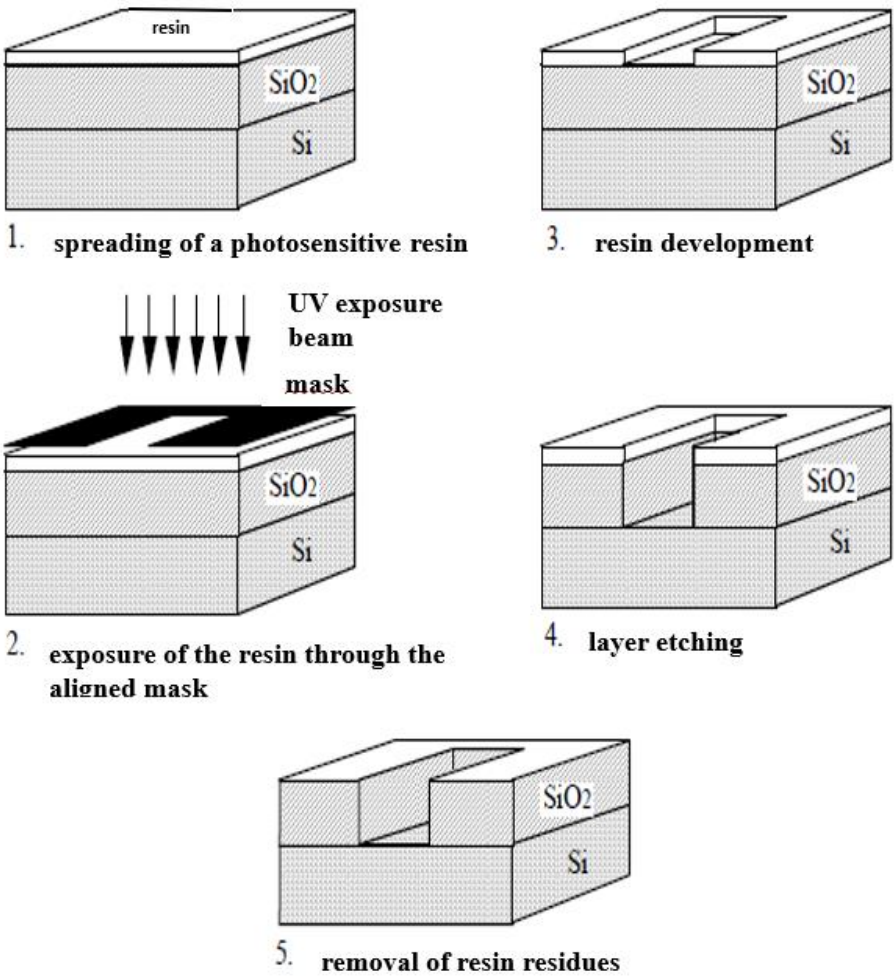



Fig.VI.2 The photolithography process in PN junction

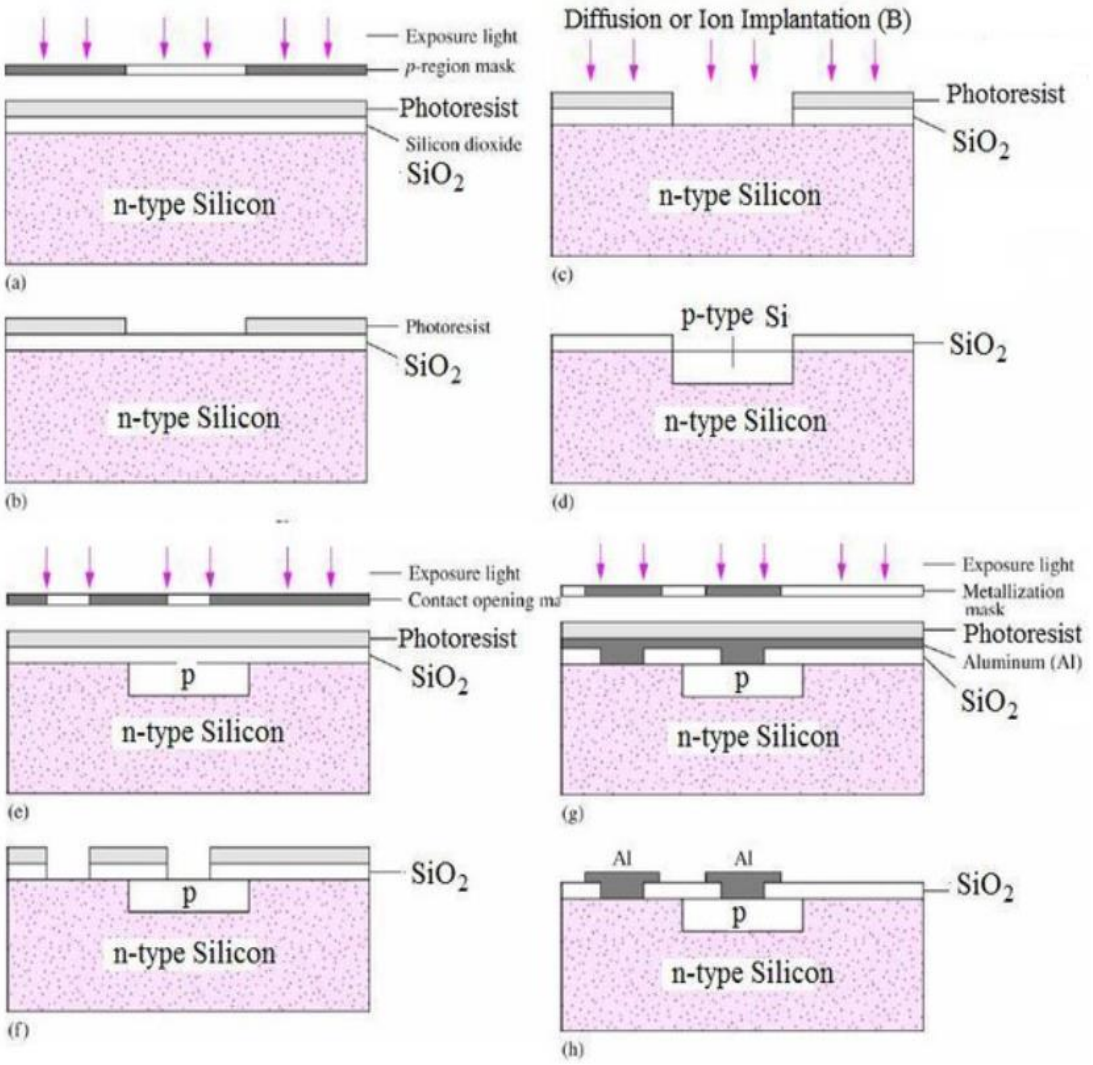



Fig VI.3 Planar technology of P-N junction diodes.

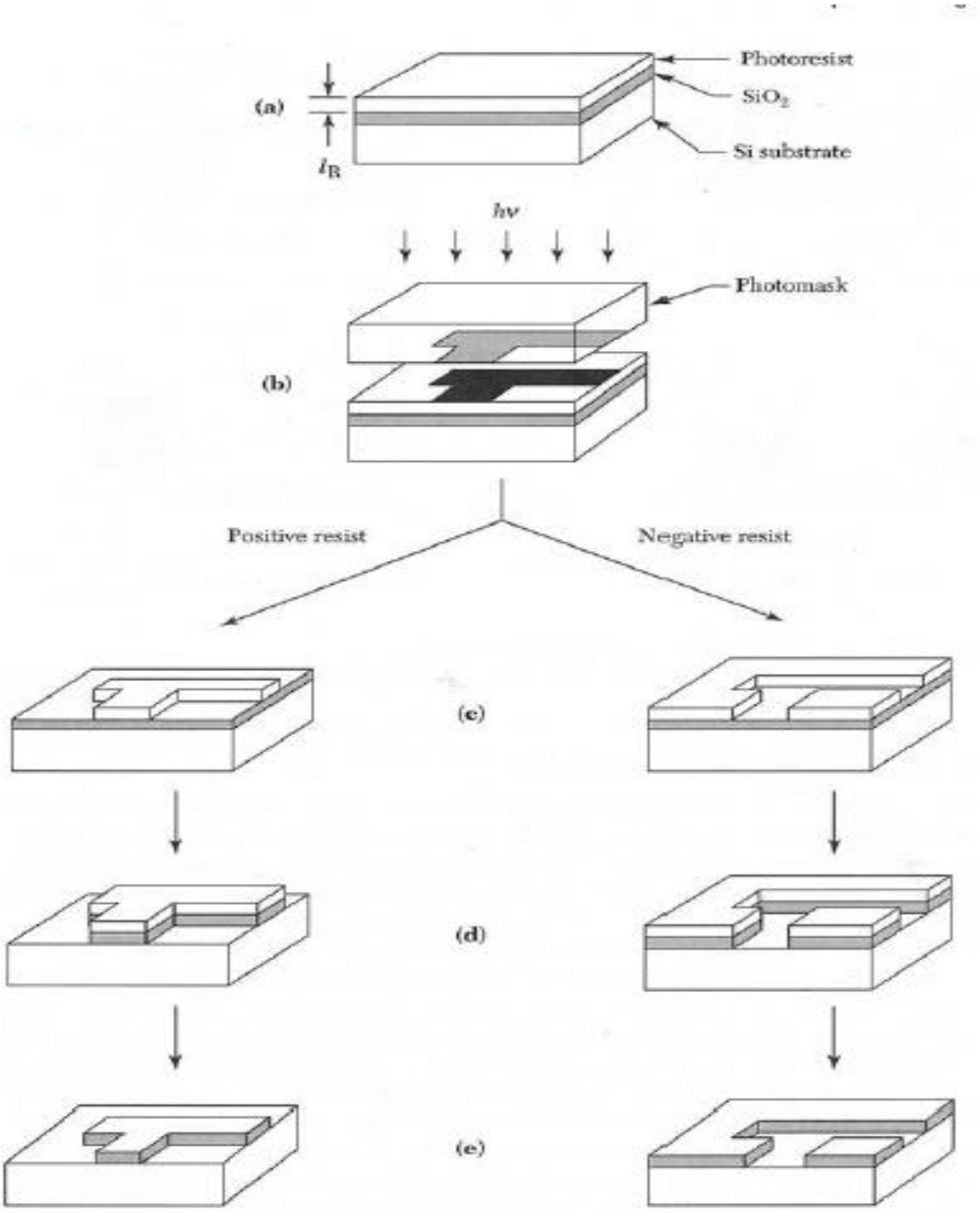



Fig.VI.4 Resin negative and positive

**Creating a pattern on a plate:**

Similar to photographic techniques, two types of photosensitive resin can be used:

- positive resin,
- negative resin.

In the case of a positive resin, after the operation, the engraved layer of the wafer will have exactly the same pattern as the original mask. For example, a metal pattern on the mask (corresponding to an opaque pattern) will correspond to the same oxide pattern remaining on the wafer after etching.

In the case of a negative resin, the complementary pattern is obtained on the wafer.

The resin is spread using a centrifugation technique. This involves using a turntable (Fig VI.5 and VI.6) which sucks in the wafer to prevent it from being ejected and, by adjusting the rotation speed (to approximately 4,000 rpm) and acceleration, spreads the resin evenly.

DRYING THE RESIN: 2 minutes 30 seconds on a hotplate at 120°C.

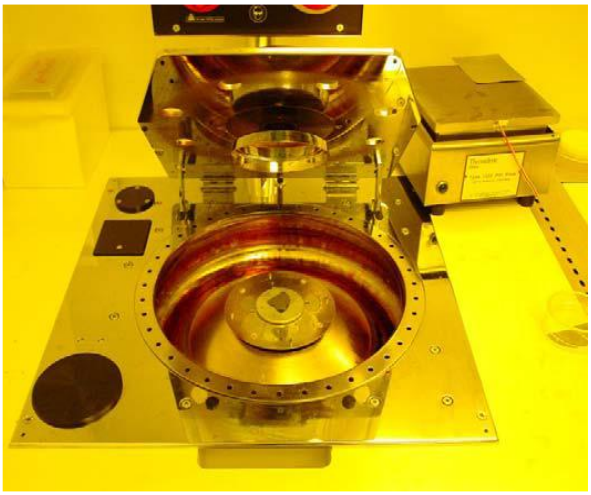
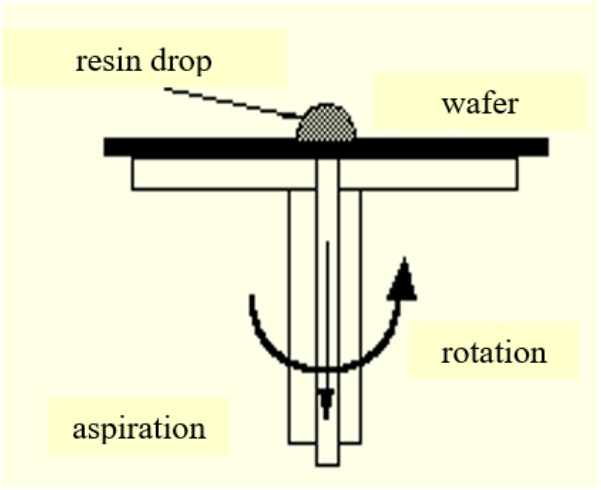


Fig.VI.5 Turntable for spreading photosensitive resin. The rotation speed is calculated to obtain a thin layer over the entire surface with a constant thickness.




FigVI.6. Spreading resin on wafers: 'spinnerets'

Fig VI.7 details the photolithography operations. In the case shown, the oxide is the negative of the chromium dioxide pattern of the mask. The resin is referred to in this case as the negative.

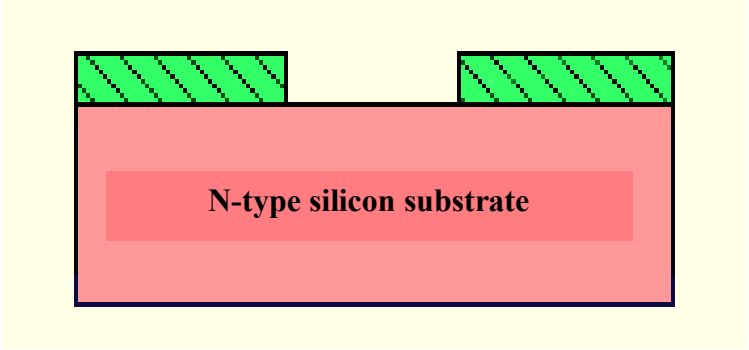



Fig VI.7 Principle of photolithography. The mask pattern has been transferred to the plate. The resin is negative in this case.

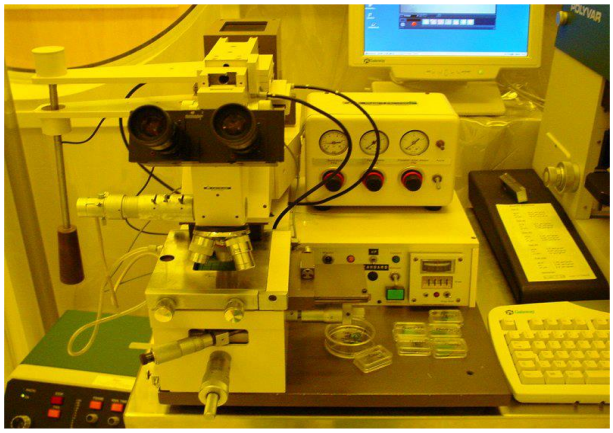
**VI.3 Sunstroke and its limits**

The exposure of the plate can be carried out in different ways:

- by contact,
- by proximity,
- by projection,

As shown in Fig VI.8 . Each of these techniques has its advantages and disadvantages. For example, the contact technique theoretically provides the best pattern definition, but damages the mask after each masking operation due to significant friction at the microscopic scale.

Projection gives the least good optical definition, due to the effects of light diffraction, but on the other hand allows for a reduction; in this latter case, the manufacture of the mask is simpler since it does not require a definition at least equal to that of the pattern transferred onto the plate.



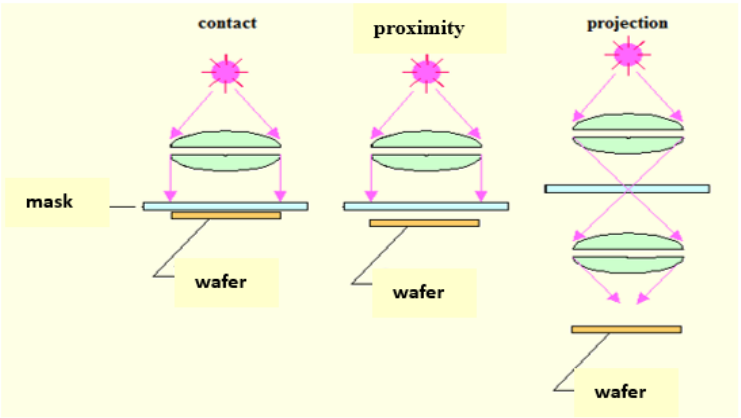



Fig VI.8 : different exposure techniques: contact, proximity and projection.

**Exercise :** Give the correct answer below;( The correct answer is in italics)

1. A photosensitive resin is

a. a resin that is transparent to ultraviolet light

*b. a resin that polymerizes under the action of radiation, preferably ultraviolet radiation*

c. a resin that is opaque to ultraviolet light and polymerizes under the effect of infrared photons

d. a resin that is sensitive to photomasked patterns

2. Irradiation is generally in the ultraviolet wavelength range

*a. to work in the visible range and irradiate with minimal diffraction spots*

b. to avoid the influence of heating the wafer, which emits in the infrared range

c. to obtain diffraction spots that are large enough to illuminate the entire wafer

d. to sanitize the clean room by attacking bacteria

e. to reduce the duration of exposure to sunlight and sterilize the clean room

3. Photolithography consists of:

*a. applying photosensitive resin, exposing it to light, etching the layer to be engraved, developing the resin and stripping it off.*

b. Applying photosensitive resin, exposing it to light, developing it, stripping off the resin and etching the layer to be engraved.

c. applying photosensitive resin, exposing it to light, developing it, etching the layer to be engraved, and stripping the resin

d. exposing photosensitive resin to light, applying it, developing it, etching the layer to be engraved, and stripping the resin

4. The definition of the insolated pattern is optimal for insolation.

a. by projection with a ratio of 1

b. by projection with a ratio of 5

c. by proximity

*d. by contact*

5. In submicron technologies, exposure is preferred

a. by proximity because the definition is better

*b. by projection and reduction to manufacture masks at scale 5*

c. by contact because the masks must be the same size as the patterns

d. by projection and enlargement because the definition is better with a ratio of 5

# Chapter VII : Etching and Chemical-Mechanical Polishing (CMP)

## VII.1 Etching

### 1.1 Introduction

Following on directly from lithography, engraving is sometimes associated with this process under the name lithogravure.

Two techniques are commonly used:

- Wet Etching,
- Dry Etching..

### 1.2 Wet Etching:

Initially, etching was carried out by chemical attack in a wet environment. Oxides are generally etched by bases or acids (hydrofluoric acid HF for silica). The main properties of chemical attack are:

– very high **selectivity**, which is linked to the choice of chemical agents used to stop the attack at the interface between two different layers,

– **isotropy**, which leads to poor definition of the pattern to be etched, particularly in lateral etching. On the other hand, the resulting profile is favorable for the continuity of the deposition of the upper layers.

In many technological fields, wet etching is widely used because it is relatively simple to implement and, in large tanks, a complete batch of up to 200 wafers can be processed in a single operation.

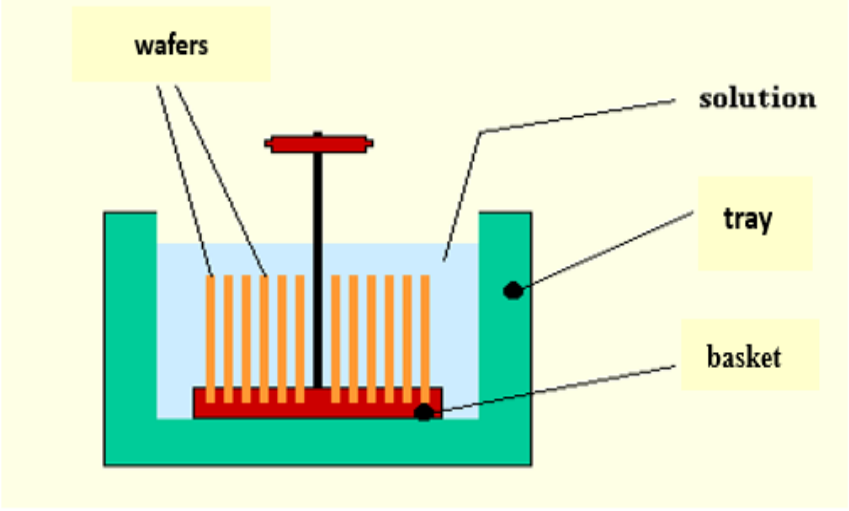



Fig. VII.1 Etching of a wet-process wafer basket.

Wet etching has certain disadvantages, namely:

– Etching is isotropic (all directions in space), which creates lateral attacks, particularly in areas protected by resin.

– The etching speed depends on the concentration and type of impurity contained in the film to be etched. This etching speed depends on the quantity of substrates treated, with etching efficiency decreasing after several batches.

– The end point of etching is difficult to control. This can lead to lateral or vertical over-etching in the case of low selectivity.

**1.3 Dry Etching:**

Dry etching is actually a plasma etching technique that involves both ion bombardment effects and chemical reactions. It is known as R.I.E. (Reactive Ion Etching).

The reactor resembles the horizontal substrate-holding platinum deposition reactor, but in this case the injected gases are used to etch the surface layer (see Fig. VII.2).

Similarly, a radiofrequency generator is used to generate reactive species in the reactor.

The principle of the process, shown in the figure opposite, can be summarized as follows:

- generation in the plasma of species that can chemically attack the layer,
- transfer of reactive species from the plasma to the surface of the layer to be etched,
- adsorption of the attacking species on the surface,
- reaction with the surface material.

The material produced by the reaction must be volatile in order to leave the surface.

- desorption of the reaction product,
- diffusion into the gaseous environment.

If all these conditions are met, we can expect to obtain a good plasma etching result. It should be noted that the difficulty in developing this technological step lies in generating volatile species after surface reaction.

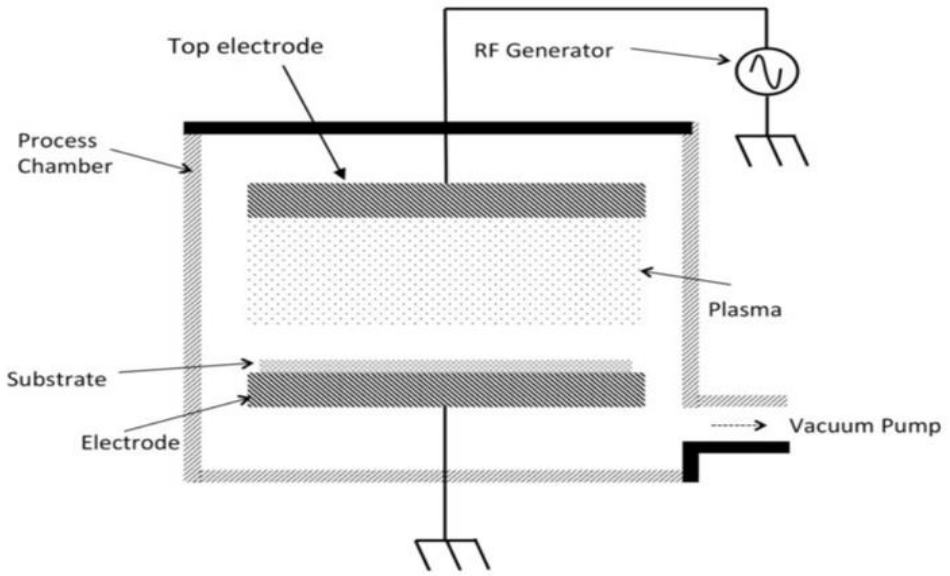



Fig. VII.2 Plasma etching reactor with horizontal substrate holder plate. The substrate is positioned on the bottom electrode that is electrically grounded and the top electrode is connected to a RF generator

Dry etching processes were introduced more recently to solve the problems of isotropy and contamination posed by wet etching. This is a necessary step in order to access increasingly dense technologies with greater quality control. The type of etching must therefore be chosen according to the dimensions of the patterns to be reproduced. With an isotopic wet chemical etching system, the etching result is unacceptable as soon as the dimensions of the patterns are of the same order of magnitude as the thickness of the etched layers.

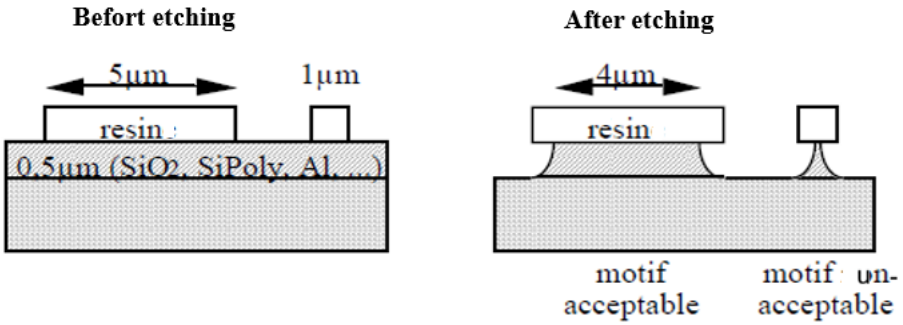



Fig.VII the problems of isotropy and contamination posed by wet etching

In practice, the difference between isotropic and anisotropic etching can be illustrated in the following figure. It is important to take into account the greater lateral etching that occurs with wet etching. Clearly, anisotropic etching is preferable for very small patterns.

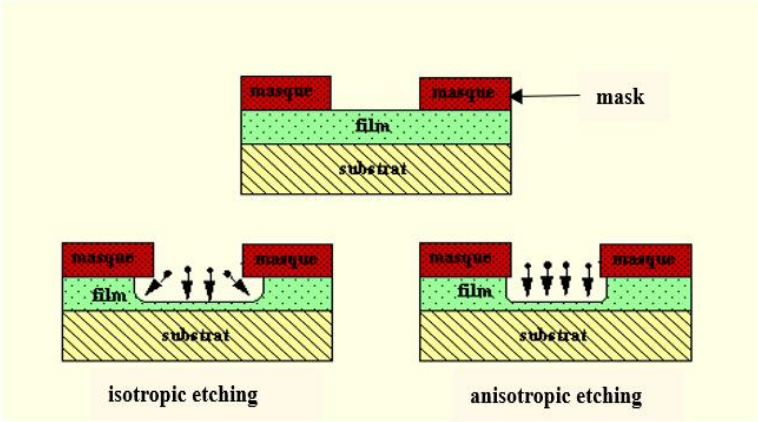



Fig VII.3 Difference between isotropic and anisotropic engraving. The width of the engraved pattern will be different.

**VII. 2- Surface Polishing**

Polishing is an essential step in preparing substrates for epitaxial growth processes. It produces a flat, clean surface free of defects, ensuring optimal quality of the deposited layers.

**2.1 Objectives of polishing**

• Reduce surface roughness.

• Remove impurities and surface defects.

• Ensure uniformity across the entire surface of the substrate.

**2.2 Polishing methods**

• Mechanical polishing: use of abrasives to gradually reduce irregularities.

• Chemical-mechanical polishing (CMP): combination of mechanical action and chemical reactions to obtain a perfectly smooth surface.

• Chemical polishing: selective dissolution of the surface using suitable chemical agents.

**Expected results:**

• Uniform, shiny surface.

• Improved crystalline quality of epitaxial layers.

• Reduction in defects related to subsequent growth.

**2.3 Chemical-mechanical polishing (CMP):**

Chemical mechanical polishing (or planarization) is the most popular technique for removing the surface irregularities of silicon wafers. Typical CMP slurries consist of a nano-sized abrasive dispersed in an acidic or basic solution. A chemical reaction softens the material during mechanical abrasion. The abrasive particles have a size distribution that directly affects critical metrics, including rate of removal and wafer defects. Particle size analysis is therefore a key indicator of CMP slurry performance.

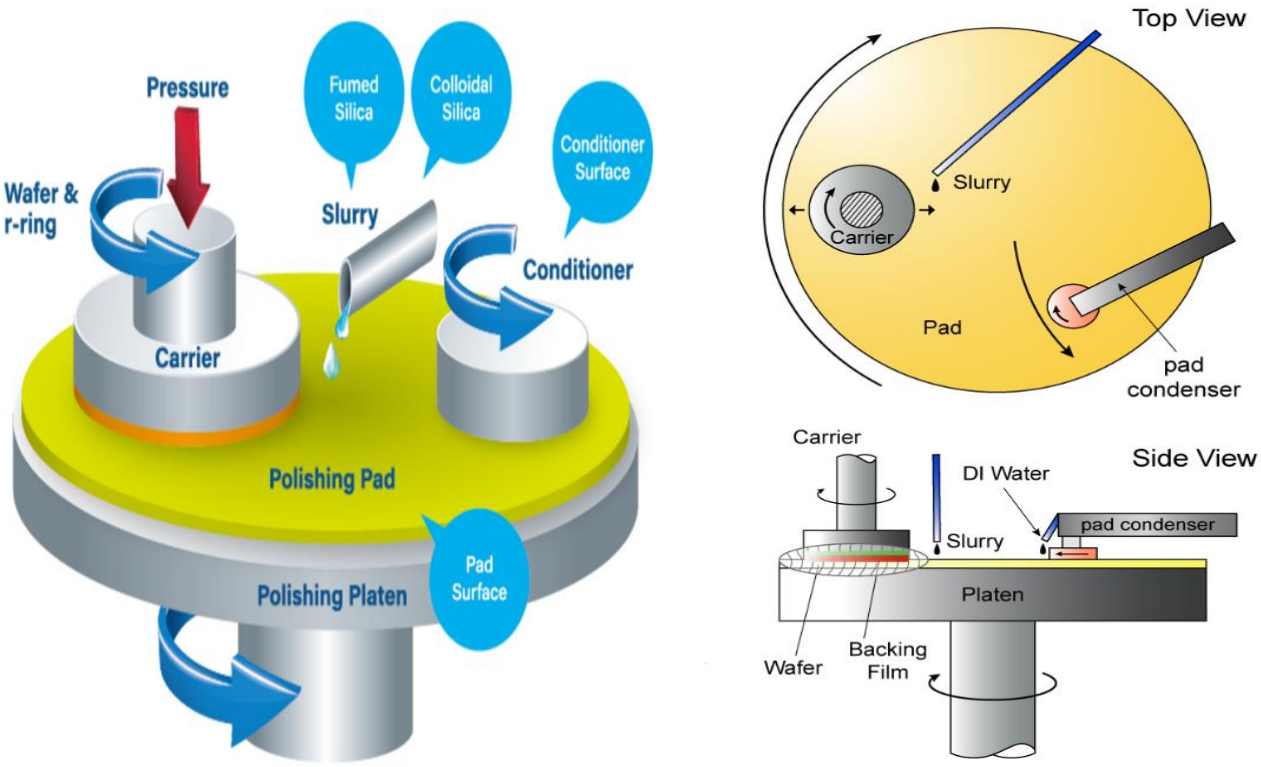



Fig.VII.4 Overview of the chemical-mechanical planarisation process in the semiconductor manufacturing industry

**Exercise:** Give the correct answer below;( The correct answer is in italics)

1. Wet etching is

a. anisotropic because it mainly attacks laterally

*b. isotropic*

c. anisotropic because it mainly attacks perpendicular to the wafer surface

d. anisotropic because it only attacks in a predefined crystallographic direction

2. Plasma etching is

*a. anisotropic because it preferentially attacks perpendicular to the surface*

b. isotropic because it preferentially attacks perpendicular to the surface

c. anisotropic because it preferentially attacks parallel to the surface

d. isotropic because it attacks in all directions in space

3. To create a spacer:

a. wet etching is used to remove a deposited oxide layer

b. isotropic dry etching is used to remove a thermal oxide layer

c. reactive ion etching is used to remove a silicon layer

*d. anisotropic etching is used to remove a thermal or deposited oxide layer*

# Chapter VIII : Métallization and Passivation

## VIII.1 Introduction

In the manufacture of semiconductor devices, the metallization and passivation stages play a crucial role.

- Metallization ensures electrical connection between the different active regions of the component.
- Passivation protects the device from external aggressions (moisture, mobile ions, contamination).

These processes guarantee the reliability, performance and longevity of integrated circuits.

## VIII 2. Metallization

### 2.1 Objectives

- Create ohmic contacts between the doped regions and the electrodes.
- Ensure reliable interconnection between the various circuit components.
- Minimise contact resistance and electrical losses.

### 2.2 Materials used

- Aluminium (Al): the most common material, easy to deposit and etch.
- Copper (Cu): used in advanced technologies for its low resistivity.
- Alloys and diffusion barriers: TiN, W, $CoSi_2$, to prevent metal migration.

### 2.3 Deposition techniques

This operation is necessary when a conductive, insulating or masking layer needs to be created in a process that does not directly use the substrate material. For example, if silicon oxide is required when the substrate and/or underlying layer are not made of silicon (this could be a metal layer or a silicon nitride layer, for example), the only solution is to deposit oxide (or another type of insulator). This is because thermal oxidation is no longer possible and deposition must be carried out. This is done in a furnace or rack that contains all the components of the layer to be produced.

The deposition techniques that will be used to deposit a layer of insulator or oxide will most often be very general, allowing layers of other materials such as metals or even semiconductors to be produced.

Several deposition techniques are industrially feasible:

• Thermal evaporation: deposition by heating and condensation of the metal.

• Cathodic sputtering: bombardment of a metal target with ions.

• Chemical vapour deposition (CVD): used for certain refractory metals.

### 2.3.1 Thermal evaporation:

The thermal evaporation technique is very simple and consists simply of heating a material by the Joule effect, which, when vaporised, will deposit on the substrates. The material to be deposited is placed in a crucible (made of tungsten). This technique is particularly suitable for depositing aluminium, as the evaporation temperature of this metal is lower than the melting temperature of the crucible (made of tungsten). The following figure shows the principle behind this technique; the setup is similar to that used in electron beam deposition. In order to improve the homogeneity of the deposited layers (very slight variations in thickness), the substrates are constantly moved. In the case of the setup shown below, the substrate holder rotates.

A quartz balance is used to control the thickness of the deposited layers. The principle behind this is to detect the drift in the quartz's oscillation frequency caused by the change in its mass during the growth of the deposited layer (the deposit is also made on the quartz). This is therefore an electrical measurement that must obviously be calibrated. At the start of each experiment, the reference frequency is redefined. By measuring the frequency shift over time, it is also possible to determine the growth rate of the deposited layers.

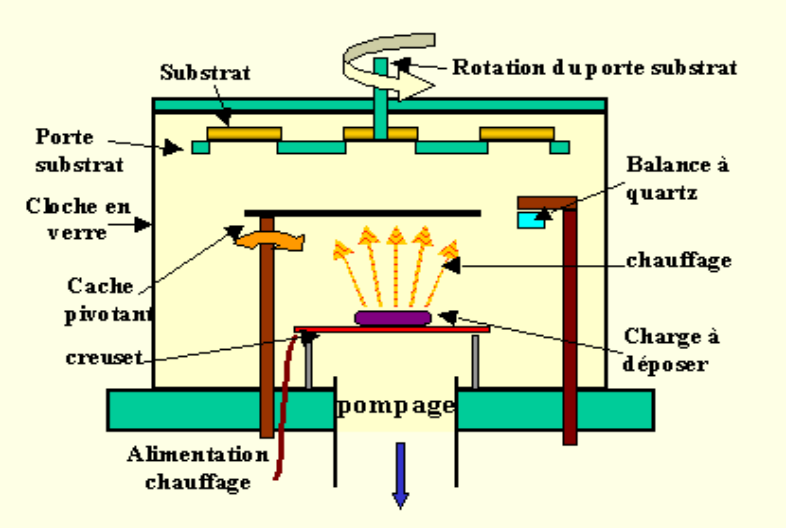



Fig. VIII.1 Evaporation deposition chamber. The crucible containing the material to be deposited is heated by the Joule effect.

### 2.3.2 Cathodic sputtering:

The principle of cathodic spraying, also known as "sputtering", is to use the energy of a plasma (partially ionised gas) on the surface of a target (cathode) to remove atoms from the material one by one and deposit them on the substrate.

To do this, plasma is created by ionising a pure gas (usually argon) using a potential difference (DC or pulsed DC) or electromagnetic excitation (MF, RF). This plasma is composed of $Ar^+$ ions that are accelerated and confined around the target by a magnetic field. Each ionised atom, upon striking the target, transfers its energy to it and strips away an atom, which has sufficient energy to be projected towards the substrate.

Plasma is created at relatively high pressures ($10^{-1}/10^{-3}$ mbar), but it is necessary to start at a lower pressure before introducing argon to avoid contamination from residual gases in the chamber.

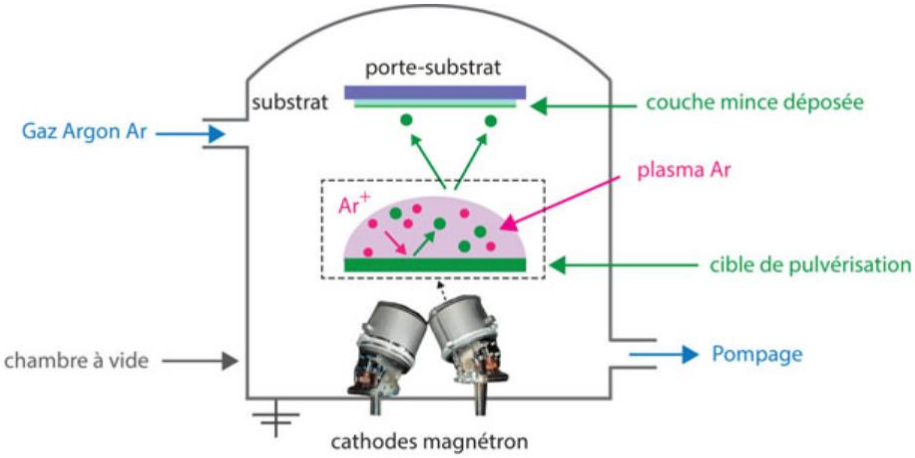



Fig. VIII.2 Diagram of the principle of cathodic spraying (sputtering)

### 2.3.3 Chemical vapor deposition (CVD):

CVD techniques are used to grow layers of insulators or polycrystalline silicon. They are generally carried out in a furnace into which the reactants are introduced. Depending on the deposition pressure values, the quality of the layers (structural and electrical properties) can be modified. Low-pressure techniques (L.P.C.V.D.) enable the deposition of polycrystalline silicon, the use of which in technological processes has led to a significant improvement in integration (self-alignment of MOS transistor grids or bipolar transistor emitters, interconnections, dopant sources, Fig VIII.3.).

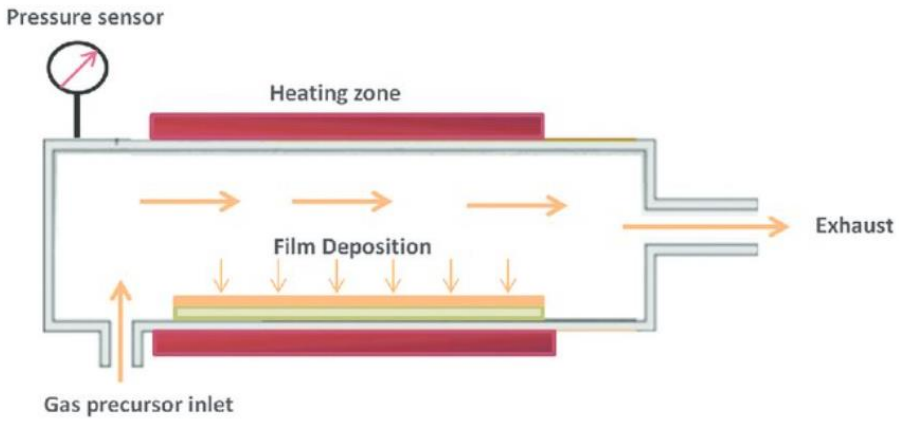



Fig. VIII.3 Schematic diagram of a chemical vapor deposition (CVD) system

**2.4 Problems and solutions**

- Metal diffusion into silicon → use of barrier layers.
- Electromigration → selection of resistant materials and optimization of line geometry.

**VII. 3. Passivation**

**3.1 Objectives**

- Protect the semiconductor surface from oxidation and moisture.
- Reduce the effects of parasitic charges and mobile ions.
- Improve the electrical and thermal stability of the device.

**3.2 Materials used**

- Silicon dioxide ($SiO_2$): conventional insulator, good chemical protection.
- Silicon nitride ($Si_3N_4$): effective barrier against moisture and sodium ions.
- Advanced polymers and oxides: used in modern technologies for greater flexibility.

**3.3 Deposition techniques**

- CVD (Chemical Vapor Deposition): uniform deposition of $SiO_2$ or $Si_3N_4$.
- PECVD (Plasma Enhanced CVD): improves film quality at low temperatures.
- Thermal oxidation: formation of a $SiO_2$ layer directly on silicon.

**3.3.1 PECVD (Plasma Enhanced CVD): improves film quality at low temperatures.**

PECVD deposition is therefore based on the creation of species or elements to be deposited at low temperatures through the supply of energy in electromagnetic form (usually a radiofrequency source). This technique therefore avoids high-temperature stages that can lead to the redistribution of dopants, for example. However, in order to improve the quality of the deposited layers, it is

necessary to heat the substrates "slightly" (possibly by a few hundred degrees). Industrially, two types of furnace are available, their basic designs being shown in the following two figures:

- horizontal substrate holder platinum furnace,
- "hot wall" furnace.

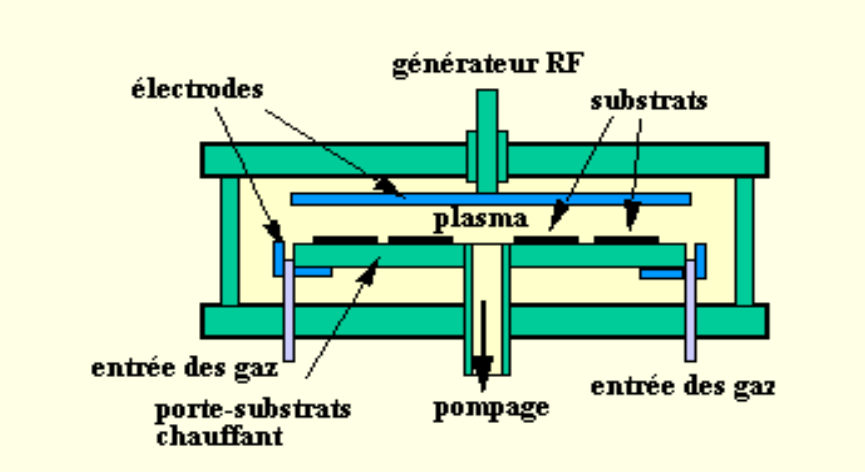



Fig. VIII.4 Plasma reactor with horizontal substrate holder plate

**4. Importance in integrated circuits**

- Metallization enables complex interconnection networks to be created in modern chips.
- Passivation ensures long-term reliability by protecting against electrostatic discharge and corrosion.
- Together, these processes ensure the performance and durability of electronic devices.

**Exercise:** Give the correct answer below;( The correct answer is in italics)

1. Sputter deposition involves

a. sending electrons to a target electrode

*b. removing ions from a target using a plasma of neutral gas ions sent towards the substrate*

c. creating a chemical reaction in a plasma to deposit the species onto a substrate

d. creating a reactive ion plasma to sputter the substrate

e. sputtering by heating the target electrode, which sends ions onto the substrate

2. An oxide can be deposited

a. by thermal evaporation assisted by oxygen injection

b. by reactive plasma etching

*c. by plasma-assisted chemical vapour deposition*

d. by thermal evaporation

3. A refractory metal coating can be applied.

a. by thermal evaporation

b. by low-pressure chemical vapour deposition

c. by atmospheric pressure chemical vapour deposition

*d. by electron beam sputtering*

**Conclusion**

Metallization and passivation are two complementary and essential steps in the microfabrication of semiconductors.

- Metallisation establishes electrical connections.
- Passivation protects and stabilizes the device.

Mastering these processes is essential to meet the requirements of modern microelectronics: miniaturization, reliability and high performance.

# General Conclusion

This module, devoted to ***semiconductor device fabrication processes***, provides a comprehensive and structured overview of the various technological steps involved in transforming raw silicon into functional electronic components. Through the study of purification, crystal growth, epitaxy, doping, oxidation, photolithography, etching and metallization, students gain an in-depth understanding of the physical and chemical mechanisms involved in each process. The focus is on planar technology, which forms the basis of modern integrated circuit manufacturing. The course also highlights technological constraints, clean room requirements and the importance of controlling manufacturing parameters to ensure device performance and reliability. This modest teaching aid thus provides a general foundation in semiconductor device manufacturing for further advanced studies and a future career in microelectronics.

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