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Theme

Design, Implementation and Control of a Multicellular Power Converter

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Abstract

The purpose of this master project is to build a multilevel power converter with four output voltage levels, known as three cells power converter. The converter is made based on commutation cells and floating capacitors and can be used as a chopper or a half-bridge inverter.

To guarantee a good operation of the converter, a non-linear feedback is proposed based on exact input-output linearization. The controller ensures the stabilization of the voltage across floating capacitors around their references and the regulation of the output current.

Experimental results show the efficiency of the experimental setup and its control scheme in two cases: DC/DC and DC/AC structures.

Keywords: Multilevel power converter, Commutation cell, Feedback linearization, Average model, Half bridge inverter.

ملخص

أصبحت المحولات الكهربائية الساكنة أهم عنصر في أنظمة تحويل الطاقة الكهربائية الحديثة، وتحسين فعالية هذه الأنظمة وكذا مرونة عملها أدى إلى نشأة تنافس تكنولوجي وتقني شمل بنية المحولات وطرق التحكم فيها. في هذا السياق جاء هذا العمل كخطوة تجريبية لاختبار واحدة من البنى الحديثة لمحولات الطاقة والمعروفة ب " متعددة المستويات". فالهدف من هذا العمل هو انشاء محول طاقة ذو أربع مستويات لتوتر الخرج ومتكون من ثلاث خلايا. يمكنه العمل كمحول مستمر-مستمر أو محول مستمر-متناوب. لضمان عمل جيد للمحول، تم التحكم فيه باستعمال تقنية التغذية العكسية غير الخطية، والذي أدى إلى استقرار توترات المكثفات الطافية للمحول على القيم المرادة، وكذا التحكم الجيد في تغيير قيمة تيار الخرج. نتائج المحاكاة والتطبيق أظهرت مدى فعالية المحول وتقنية التحكم المستعملة في كلا الوضعين محول مستمر-مستمر، ومحول مستمر-متناوب.

الكلمات المفتاحية: محول طاقة متعدد المستويات، التغذية العكسية غير الخطية، محول مستمر-مستمر، ومحول مستمر-متناوب، المكثفات الطافية، خلية تبديل.

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General Introduction

Power electronic converters are the core of modern conversion systems and the need for improving efficiency and operation flexibility, leads to constant technical challenges around converter topologies, and control methods. [1].

Multilevel converters are one of the promising topologies which are increasingly applied in several industries as well as in renewable energy and distributed generation. However, a thorough understanding of characteristics and the operation of these topologies is mandatory in order to carry out high-performance and reliable control designs.

In this project, an adequate control of a four-level power converter, known as multicellular converter, is performed. This type of converter is built based on commutation cells and floating capacitors [2]. It can operate as DC-to-DC or as DC-to-AC converter depending on how it is wired. To test the proposed control technique on a real converter, an experimental testing bench is realized, and the control technique is implemented on it.

In order to keep the converter working correctly, its control must ensure the regulation of the capacitor voltages. Thus, the regulation allows on one hand an equal distribution of the voltage stresses on each switch, and on the other hand it provides a desired output current. To meet these control requirements, we proposed a nonlinear controller based on feedback linearization approach.

This master thesis is divided on four chapters besides the introduction and the conclusion:

- **In chapter one**, we will present the multicellular converter topology, its working principle, and the control requirements that achieve a safe and optimal operation of the converter.
- **The second chapter** is devoted to the mathematical modelling of a multicellular

converter (DC/DC and DC/AC structures). In addition, a nonlinear state feedback controller is designed in order to achieve the stabilization of the capacitors' voltages and the tracking of a reference current.

- **The third chapter** is dedicated to the presentation of the experimental setup and its main elements.
- **In the fourth chapter**, we test experimental setup under open loop control. Then, we will check the effectiveness of the linearizing feedback on controlling the multicellular converter in two versions: DC/DC and DC/AC structure.

Chapter 1

Multicellular converters

1.1 Introduction

This chapter is devoted to the description and the analysis of a multicellular power converter. This converter belongs to the category of *multilevel converters* where the output voltage has more than two levels. Moreover, this chapter presents operating principle together with the control requirements that achieve a safe and optimal operation of the converter.

1.2 Necessity of multilevel topologies

In the last decades, power electronics society has witnessed increasing challenges of powering various technological applications via switched converters as the case for electrical vehicles [3, 4], renewable energy systems [5, 6], microprocessors [7, 8], etc. In these applications, the voltage and current stress can go beyond the range that one power device can handle and unsatisfactory performances are usually faced due to the limited switching frequency.

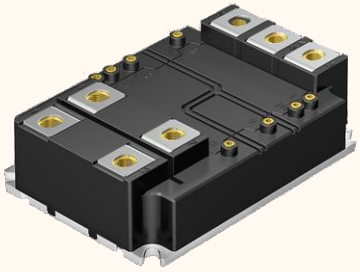
To meet the constraints in voltage or in current, several solutions have been proposed based on the association of several power converters or the connection of multiple power devices to obtain a macro-component having satisfactory characteristics in voltage and/or current [9].

Although these solutions seem to be attractive, non-straightforward synchronous control of the multiple elements must be ensured [10]. To this end, an innovative solution has been proposed at the beginning of the 1990s by H. Foch and T. Meynard using the concept

of a commutation cell [11]. The converter is named **multicellular converter** and it belongs to the class of multilevel power converters. The latter are increasingly applied in several industries as well as in renewable energy and distributed generation. However, a thorough understanding of characteristics and the operation of these topologies is mandatory in order to carry out high-performance and reliable control designs [1].

Remark 1.1:

It should be noted that modern semiconductor devices have reached high current and voltage levels. For example, the IGBT Module of Semikron (SKM450GB33F) shown below can support 3300 V and 450A.



However, using multilevel power converters with these devices can extend the power handling limits and enhance the output waveforms.

The next sections introduce the multicellular converter structure and explains how it works.

1.3 Multicellular converter description

Fig. 1.1 depicts the structure of a multicellular converter with p commutation cells. Each commutation cell is composed of pairs of complementary switches. This topology allows the share of the high input voltage E among the commutation cells by the mean of p-1 voltage sources with the following values [10]:

$$V_k = k\frac{E}{p}, \quad k = \{1, 2, ..., p-1\} \tag{1.1}$$

where V_k corresponds to the kth voltage source.

In this case, the voltage across each cell is the same and equal to E/p as shown below:

$$Vcell_k = V_k - V_{k-1} = \frac{E}{p}, \quad k = \{1, 2, ..., p\} \tag{1.2}$$

with $V_p = E$ and $V_0 = 0$.

The output voltage of the converter is given by:

$$V_o = \frac{E}{p} \sum_{k=1}^{p} u_k, \quad u_k \in \{1, 0\} \tag{1.3}$$

The DC/DC configuration of the multicellular converter offers a *p+1* output voltage levels (0, $\frac{E}{p}$, $2\frac{E}{p}$, ..., E), which makes it possible to obtain a **remarkable improvement of the output waveforms** (Low ripples and high apparent frequency), allowing a significant reduction of the filtering elements [12].

It should be noted that this converter can operate as: *chopper*, *half-bridge inverter* or *full-bridge inverter* [10]. The following figure illustrates the DC/AC version of this converter where the output voltage is given by the following expression:

$$V_o = \frac{E}{p} \sum_{k=1}^{p} u_k - \frac{E}{2}, \quad u_k \in \{1, 0\} \tag{1.4}$$

To explain the operating principle, we will consider a two cells converter for the DC/DC structure and three cells for the DC/AC structure.

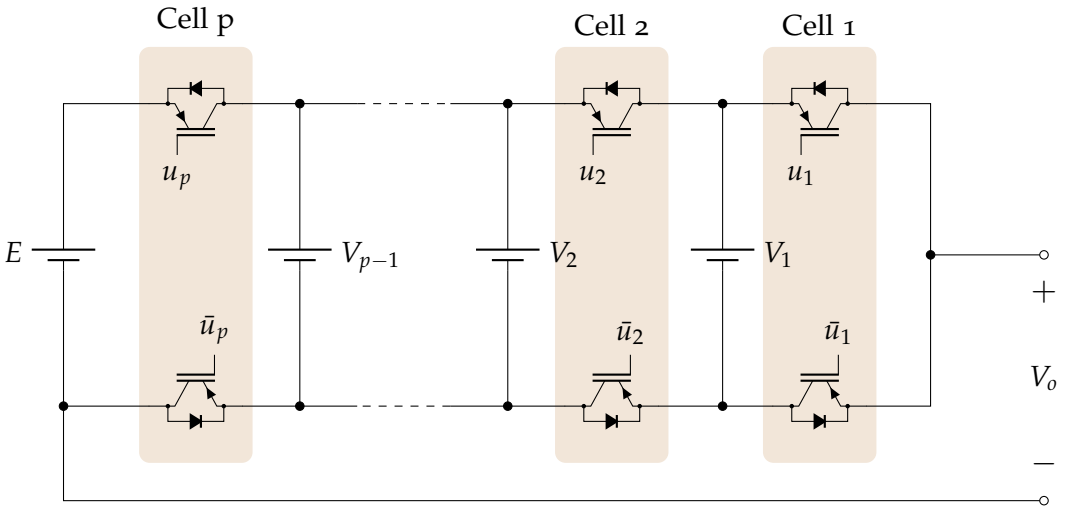


Figure 1.1: Multicellular converter with p cells (DC/DC configuration).

1.4 Operating Principle

1.4.1 Two cells chopper

In order to study the output voltage waveform in a two-cell converter and the effect of the phase shift between control signals (u_1 and u_2), we will study the chopper structure shown in Fig. 1.3.

Fig. 1.4 and Fig. 1.5 illustrates different scenarios of input signals with different phase shifts and duty cycles, and the corresponding output voltage over one switching period T_s. We have the following remarks:

1. For a zero phase shift between the control signals and whatever the duty cycle, the output voltage oscillates between 0 and E. This type of operation is therefore similar, in terms of waveforms, to the case of a chopper with a single switch (Buck converter).

2. When we slightly change the phase shift between the control signals ($\frac{\pi}{6}$), the three voltage levels (0, $\frac{E}{2}$, E) appear, whatever the duty cycle applied to the cells. The maximum amplitude of the variations is therefore always equal to E.

3. In the third case; for a phase shift of π, we remark that the amplitude of variation of the output voltage is divided by two.

   – If the duty cycle is less than 0.5, then V_o will take the values 0 and $E/2$ (See Property 2 for the general case),

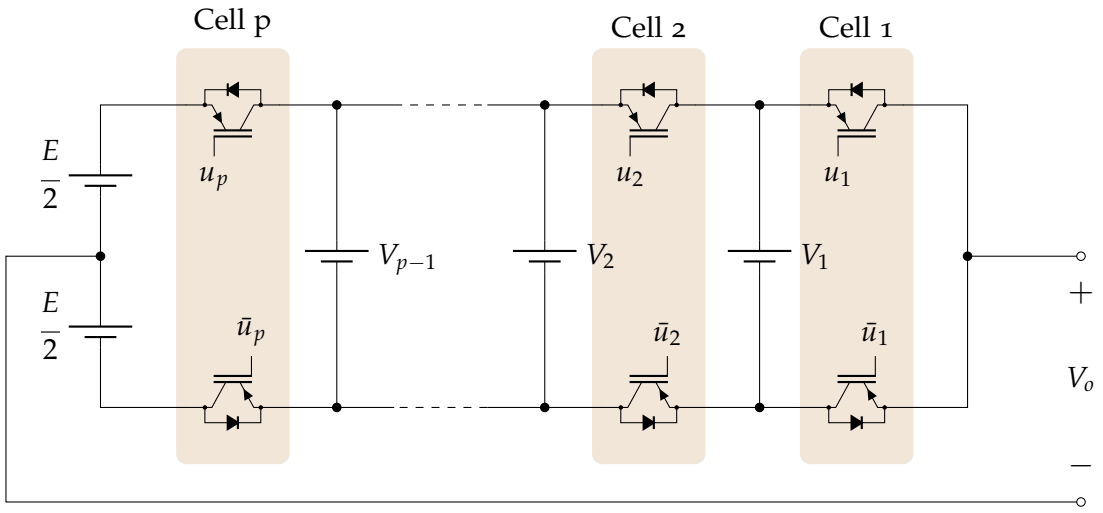


Figure 1.2: Multicellular converter with p cells (DC/AC configuration)

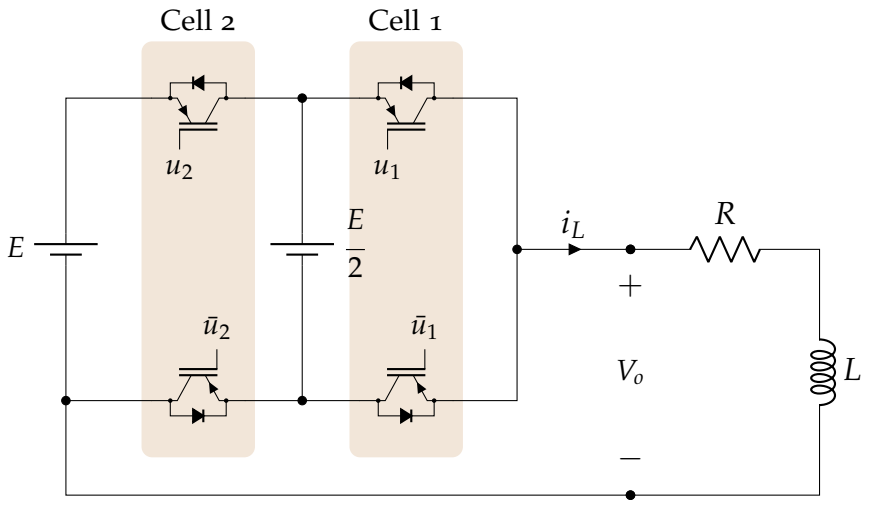


Figure 1.3: Two cells chopper connected with an inductive load.

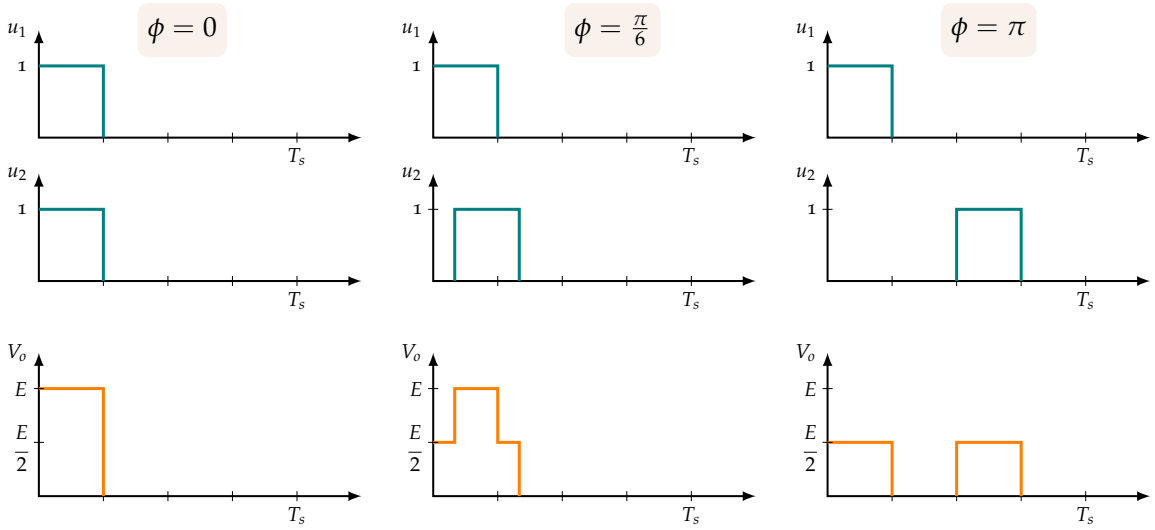


Figure 1.4: Switch signals and output voltage waveforms for 0.25 duty cycle and different phase shift values.

- if the duty cycle is greater than 0.5, V_o will take the values $E/2$ and E (Property 2).

We also note that the frequency of the output voltage waveform is doubled compared to previous cases (See Property 3 for the general case).

From the above analysis, we have also the following properties [2, 13]:

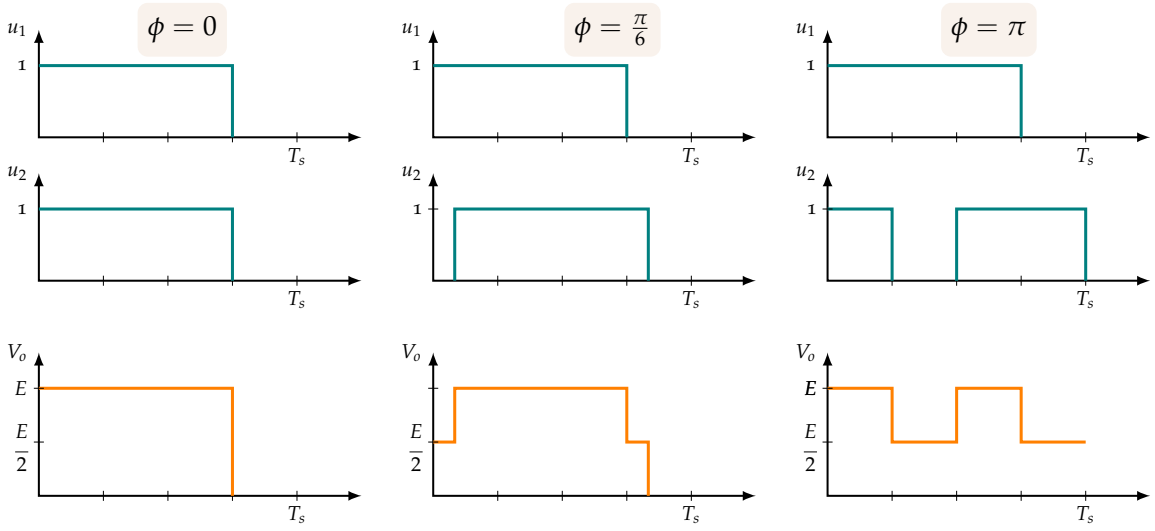


Figure 1.5: Switch signals and output voltage waveforms for 0.75 duty cycle and different phase shift values.

Property 1:

For a multicellular converter with p commutation cells, if we impose equal duty cycles of control signals and regular phase shifts of $\frac{2\pi}{p}$ between them then the output voltage ripple is divided by p.

Property 2:

For a DC/DC multicellular converter with p commutation cells, if a regular phase shift of $\frac{2\pi}{p}$ between control signals is guaranteed, and if the duty cycle is included between $\frac{i-1}{p}$ and $\frac{i}{p}$ with $i \in \{1, ..., p\}$ then the output voltage will oscillate between the levels $\frac{(i-1)E}{p}$ and $\frac{iE}{p}$ over a switching period.

For the DC/AC structure, the output voltage will oscillate between the levels $\frac{(i-1)E}{p} - \frac{E}{2}$ and $\frac{iE}{p} - \frac{E}{2}$ over a switching period.

Property 3:

For multicellular converter with p commutation cells, if a regular phase shift of $\frac{2\pi}{p}$ between control signals is guaranteed, and if duty cycles of control signals are equal then the apparent switching frequency of the output voltage is multiplied by p.

1.4.2 Three cells half bridge inverter

From the previous subsection, we have the general rules for making the best use of the multicellular structure (conditions on duty cycle and phase shift). Now, we will study the waveforms of a 3 cells inverter and perform the temporal and harmonic analysis of the output voltage waveforms.

The circuit diagram of a 3 cells half bridge inverter supplying an inductive load is shown in Fig. 1.6.

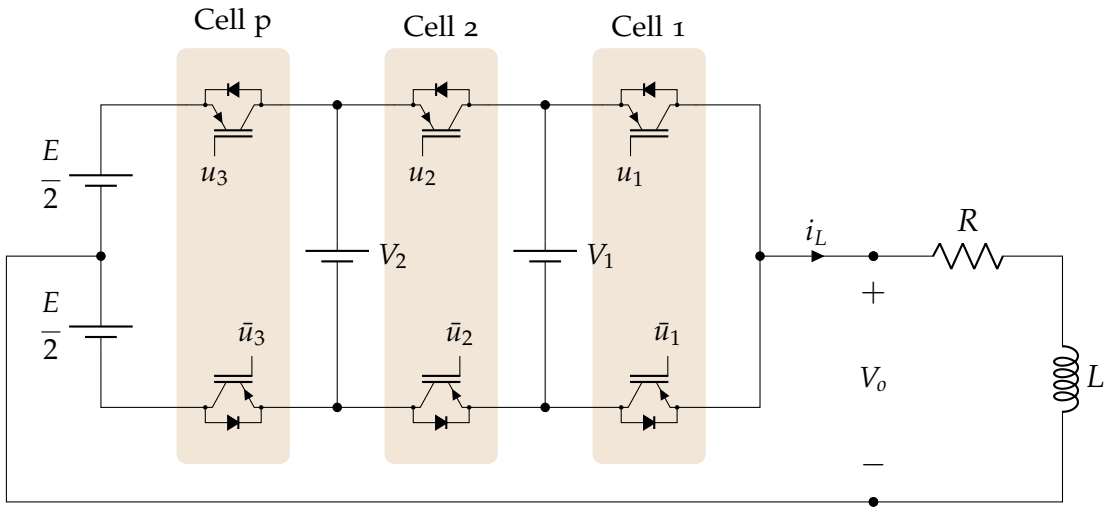


Figure 1.6: Three cells DC/AC half bridge inverter connected with an inductive load.

Case 1: Zero phase shift:

In order to investigate the effect of phase shift between control signals on the harmonic content of the output voltage, we will first study the case where all the control signals of all the cells are in phase. Let us consider a sinusoidal modulated duty cycle with a period of 10ms and modulation depth of 0.9 as shown below.

The input voltage E is chosen equal to 30V, the inductive load corresponds to $R = 10\Omega$ and $L = 2$mH, and the switching frequency equals to 10KHz.

Fig. 1.8 shows the output voltage of the inverter which oscillates between $E/2$ and $-E/2$. For zero phase shift between control signals, we remark a similar voltage waveform compared to the classical inverter.

Fig 1.9 illustrates the harmonic content of the output voltage which is normalized with

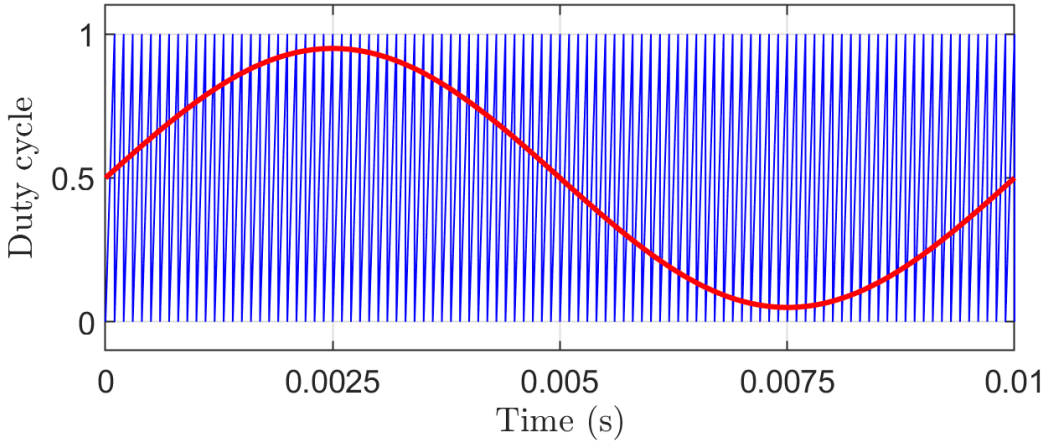


Figure 1.7: Duty cycle waveform.

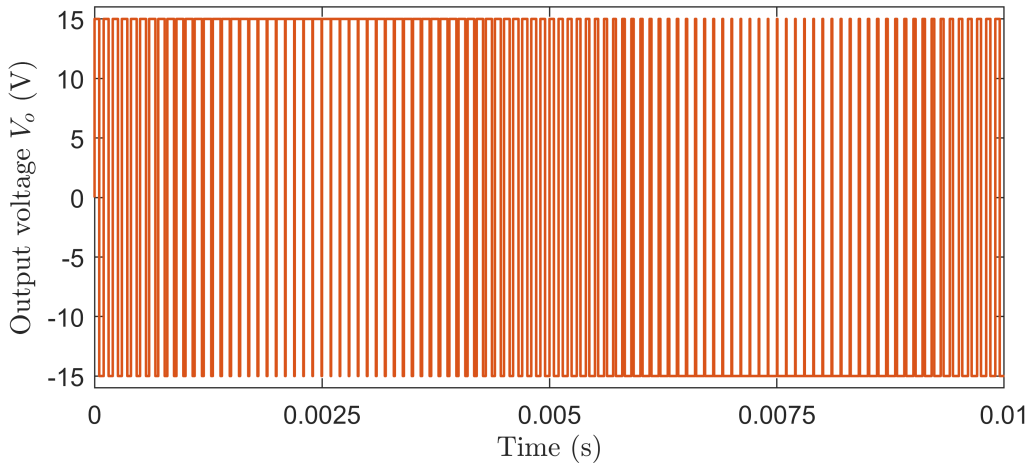


Figure 1.8: Output voltage waveform of a 3 cells inverter for a zero phase shift.

respect to the switching frequency ($f_s = 10$KHz). One can remark that different harmonic orders are present: f_s, $2f_s$, $3f_s$, $4f_s$, etc.

The load current i_L is shown in Fig. 1.10 which follows the provided duty cycle. One can observe that the current ripples are important and remarkable in this case.

Case 2: regular phase shift $\frac{2\pi}{p}$:

In this test, we will consider the same system parameters except for the phase shifts of the control signals which are chosen equal to:

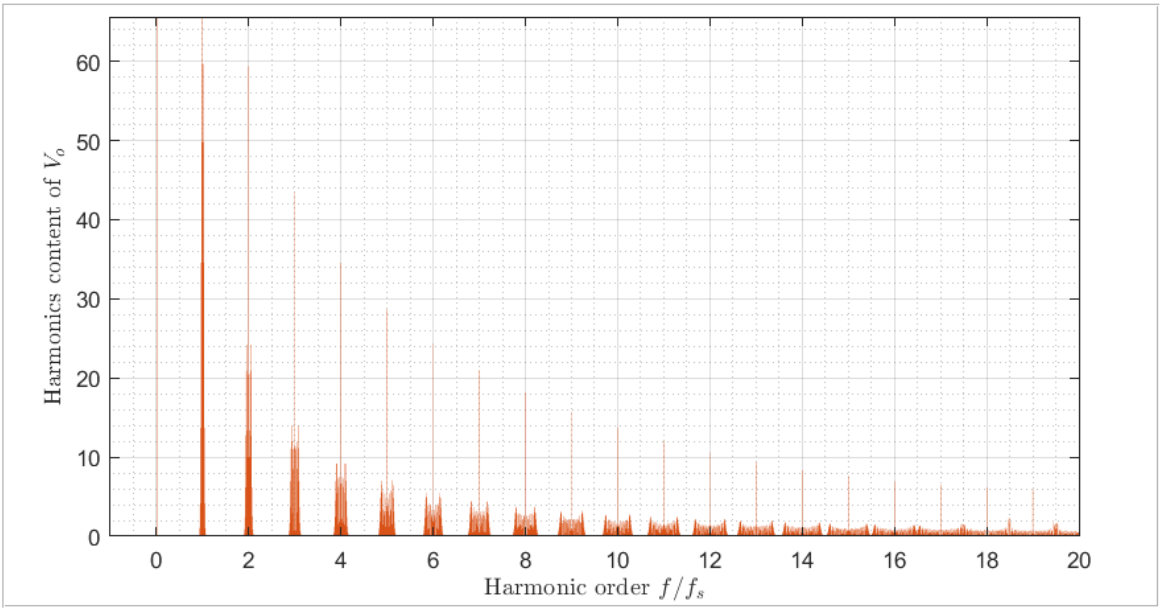


Figure 1.9: Harmonic content of the output voltage.

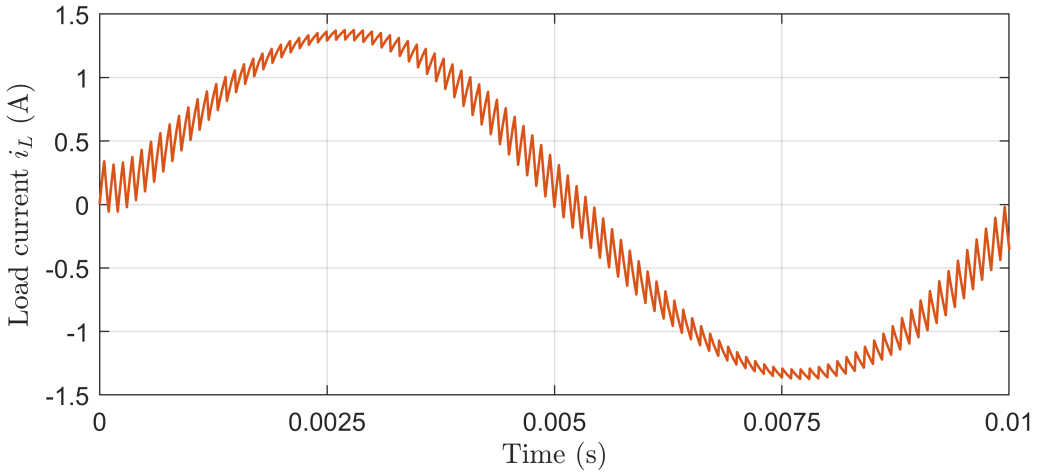


Figure 1.10: Load current i_L (zero phase shift).

$$\begin{cases} \phi_1 = & 0 \\ \phi_2 = & \frac{2\pi}{3} \\ \phi_3 = & \frac{4\pi}{3} \end{cases}$$

Fig. 1.11 illustrates the output voltage where the 4 levels are present (Property 2):

- **Level 1**: $-\frac{E}{2} = -15V$
- **Level 2**: $\frac{E}{3} - \frac{E}{2} = -5V$

- **Level 3**: $\frac{2E}{3} - \frac{E}{2} = 5V$
- **Level 4**: $\frac{E}{2} = 15V$

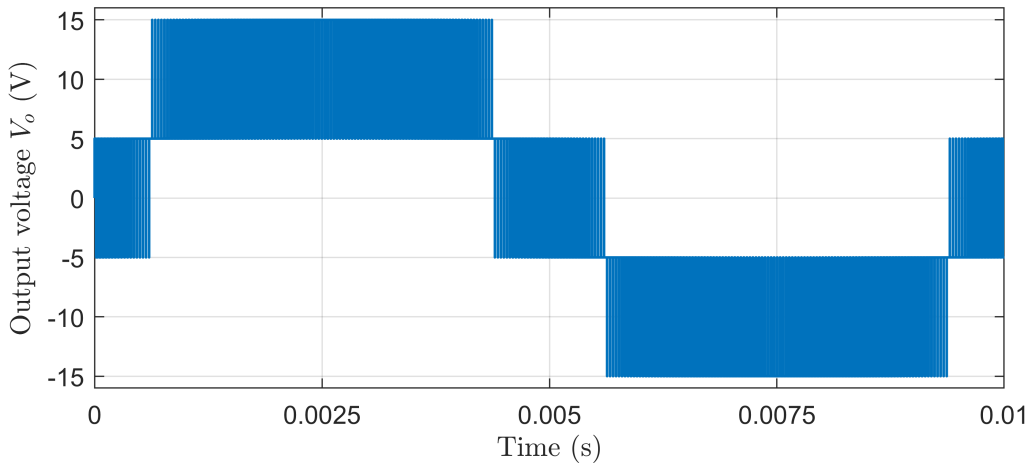


Figure 1.11: Output voltage waveform of a 3 cells inverter for a regular phase shift.

The appearance of these levels depends on the duty cycle value over a switching period (Property 2). The harmonic content of the output voltage given in Fig. 1.12 shows that only orders multiple of $3f_s$ are present ($3f_s$, $6f_s$, $9f_s$, $12f_s$, etc). This improves significantly the output waveforms and reduces and simplifies the filtering part, which is confirmed by the load current shown in Fig. 1.13. Now, we can state the fourth property of a multicellular converter.

Property 4:

For multicellular converter with p commutation cells, if a regular phase shift of $\frac{2\pi}{p}$ between control signals is guaranteed, and if duty cycles of control signals are equal then all harmonic orders are zero except multiples of p.

1.4.3 Voltage sources' variations

So far, we have assumed that the voltage sources are exactly equal to $V_k = k\frac{E}{p}$. In this subsection, we will consider the same test as before except for slight variations (5V) in the value of the voltage sources ($V_1 = 5$V instead of 10V, $V_2 = 25$V instead of 20V)

In this scenario, the waveforms remain similar to the previous ones except that the output voltage levels appearing are changed. On the other hand, the harmonic analysis of

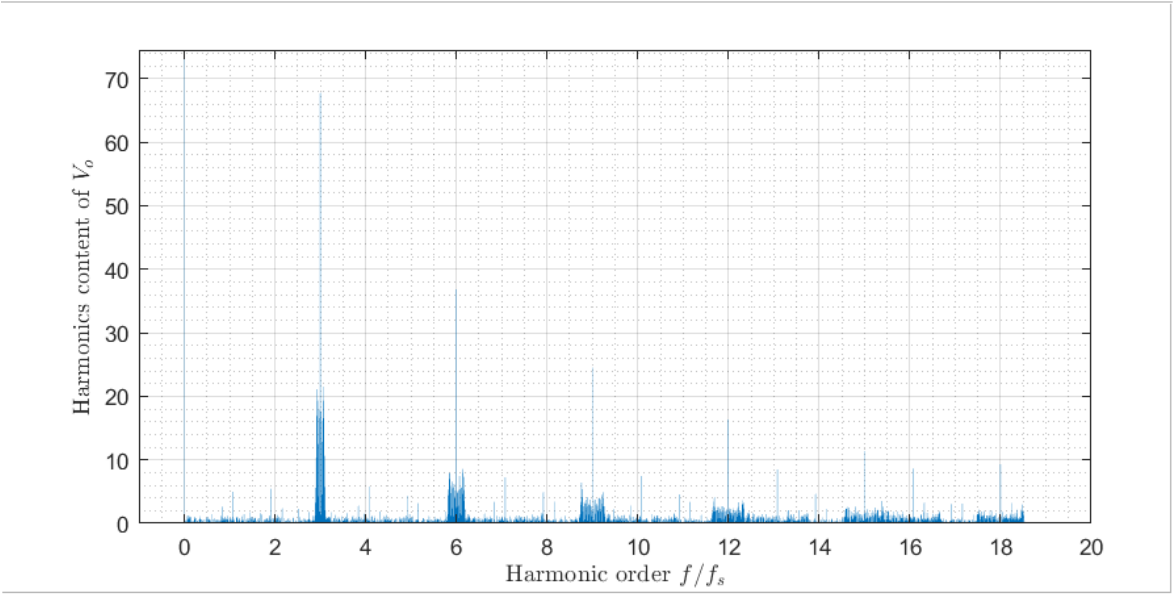


Figure 1.12: Harmonic content of the output voltage (regular phase shift).

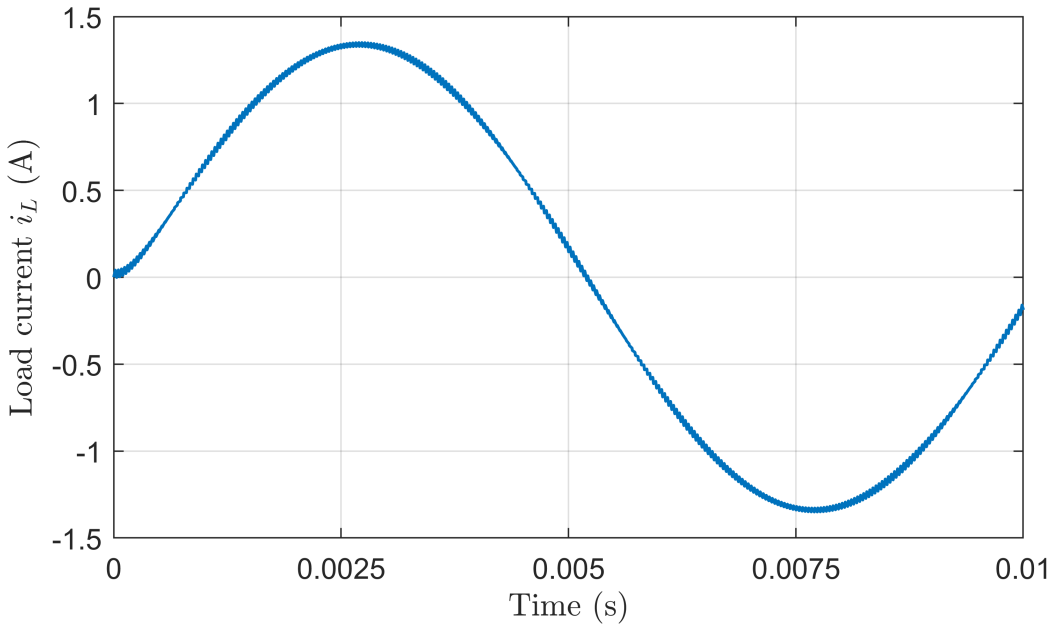


Figure 1.13: Load current i_L (regular phase shift).

V_o represented in Fig. 1.14 illustrates appearance of harmonics at all the frequencies that are multiples of the switching frequency. The amplitude of these harmonics depends on the unbalance introduced on the voltage sources.

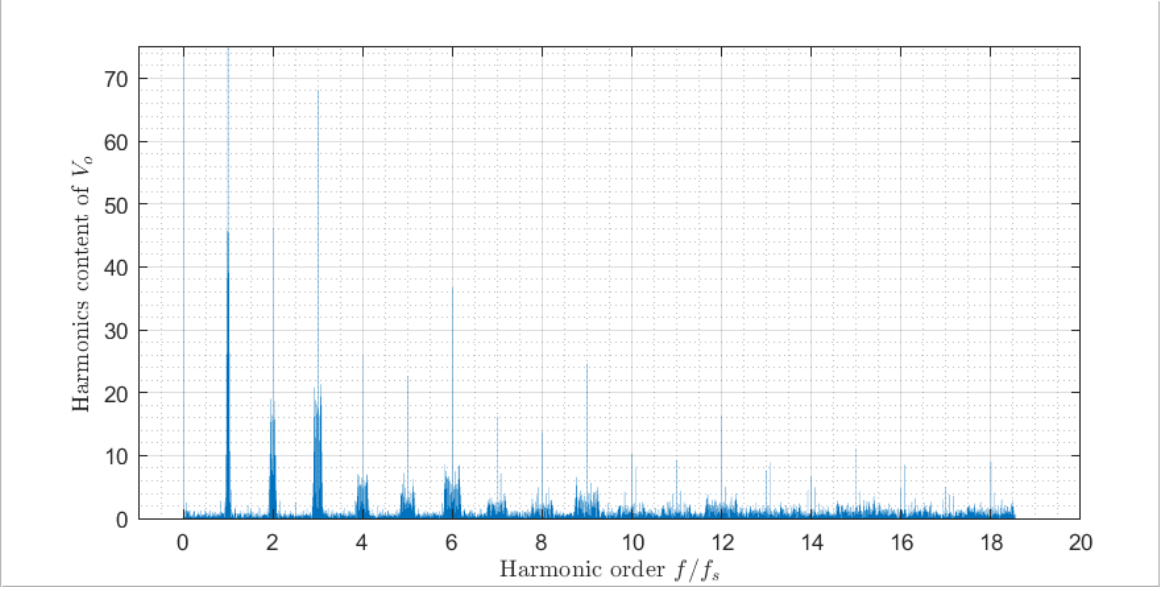


Figure 1.14: Harmonic content of V_o (regular phase shift & voltage sources unbalance).

1.5 Control requirements

In this chapter, we considered the converter topology with voltage sources. However, these sources can be replaced by capacitors (known as floating capacitors) as shown in Fig. 1.15. The control objectives of this structure are stated below.

1. The control signals have to achieve the regulation of capacitors' voltages to meet the references given by Eq. (1.1). This yields to less harmonics in the output waveforms (voltage and current) as discussed in the previous subsection.

2. In addition to the regulation of the capacitors' voltages, the control signals have to force the output current i_L to follow a reference one I_{ref} .

Remark 1.2:

For optimal operation of the converter, the phase shift between control signals has to follow the rule of $\frac{2\pi}{p}$. The latter can be easily achieved by using shifted phase modulated carriers.

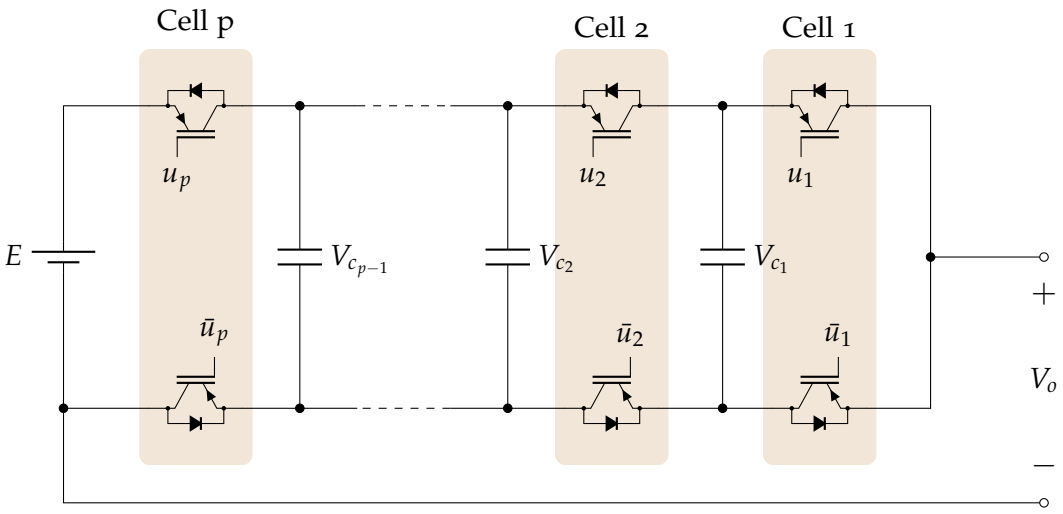


Figure 1.15: Multicellular converter with p cells and floating capacitors.

1.6 Conclusion

In this chapter, we have introduced multicellular converters as well as their main properties. One of their many advantages is the reduction of the voltage across switches. This allows the use of faster switches which, in turn, guarantee high performance. The operating principle and control requirements of the multicellular structure was described.

In the next chapter, we will present the instantaneous model as well as the average model of a multicellular converter. Then, we will present a non-linear control that forces the system to the follow control requirements.

Chapter 2

Modelling & Control of Multicellular Converter

Contents

2.1 Introduction

In this chapter, we will present the mathematical model of a multicellular converter (DC/DC and DC/AC structures) associated with an inductive load. Two models are considered: i) instantaneous model, and ii) average model. The latter will be used to design a state feedback controller in order to achieve the stabilization of the capacitors' voltages and the tracking of a reference current.

2.2 Modelling of a multicellular converter

Mathematical modelling is an essential and important phase to deal with physical systems. The multicellular converter dynamics have been described by different models in the literature such as: instantaneous model, average model, harmonic model, and hybrid model [14]. In the next subsections, we restate the instantaneous and average models of a three cells converter associated with an inductive load, as shown in Fig. 2.1. The average model will be used latter for controller design.

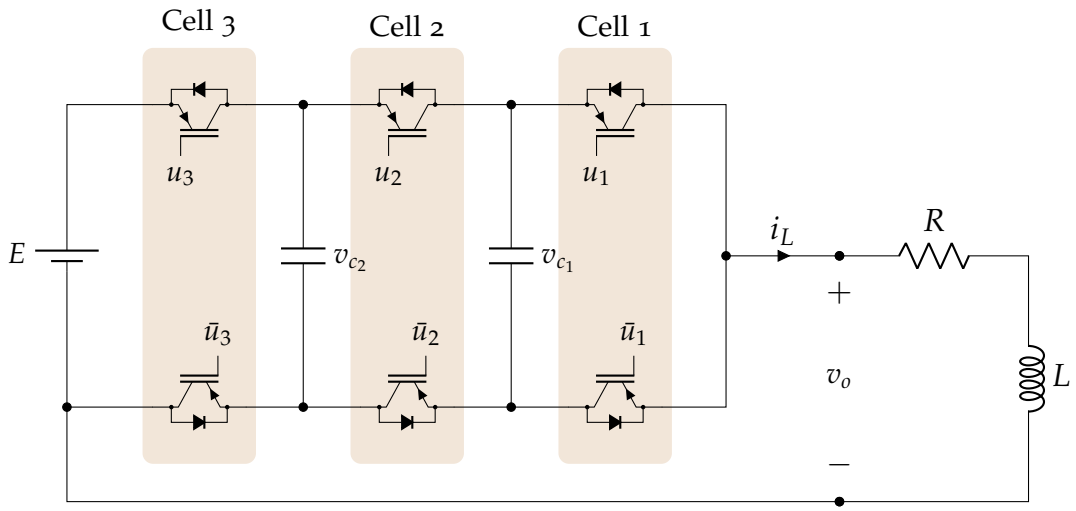


Figure 2.1: Three cells DC/DC converter associated with an inductive load.

2.2.1 Instantaneous model

The control signals in the instantaneous model are represented with their real values (0 or 1) over a switching period. Thus, the cell's state is controlled by a binary input signal $u_k \in \{0,1\}$ where $u_k = 1$ $(u_k = 0)$ indicates that the k^{th} upper switch is closed (open) and the k^{th} lower switch is open (closed). For the continous part, we distinguish two dynamics (inductor current and capacitors' voltages).

Load current dynamics:

From the converter structure, the voltage across the k^{th} cell is given by:

$$v_{cell_k} = v_{c_k} - v_{c_{k-1}}, \quad k \in \{1,2,3\} \tag{2.1}$$

with $v_{c_0} = 0$ and $v_{c_p} = E$. The output voltage of p-cells converter, denoted v_o, is given by:

$$v_o = \sum_{k=1}^{3} u_k v_{cell_k} \tag{2.2}$$

which corresponds to:

$$v_o = (u_1 - u_2)v_{c_1} + (u_2 - u_3)v_{c_2} + u_3 E \tag{2.3}$$

Therefore, the load current is described by the following differential equation:

$$L\frac{di_L}{dt} = v_o - Ri_L \tag{2.4}$$

Capacitors' voltages dynamics:

The evolution of the capacitor voltage v_{c_k} depends on the current flowing through it, which is controlled by the state of their adjacent cells:

$$i_{C_k} = (u_{k+1} - u_k)\, i_L \tag{2.5}$$

Thus, the capacitor voltage dynamic is represented by the following differential equation:

$$C_k\frac{dv_{c_k}}{dt} = (u_{k+1} - u_k)\, i_L, \quad k \in \{1, 2\} \tag{2.6}$$

Full model of three cells converter:

From (2.4) and (2.6), the instantaneous model of the converter is described as follows:

$$\begin{cases} C_1\dfrac{dv_{c_1}}{dt} &= (u_2 - u_1)\, i_L \\ C_2\dfrac{dv_{c_2}}{dt} &= (u_3 - u_2)\, i_L \\ L\dfrac{di_L}{dt} &= (u_1 - u_2)v_{c_1} + (u_2 - u_3)v_{c_2} + u_3 E - Ri_L \end{cases} \tag{2.7}$$

This model can also be rewritten in the following compact form:

$$\dot{x} = A(u)x + B(u) \tag{2.8}$$

with

$$A(u) = \begin{pmatrix} 0 & 0 & \frac{u_2 - u_1}{C_1} \\ 0 & 0 & \frac{u_3 - u_2}{C_2} \\ \frac{u_1 - u_2}{L} & \frac{u_2 - u_3}{L} & \frac{-R}{L} \end{pmatrix}, \quad B(u) = \begin{pmatrix} 0 \\ 0 \\ \frac{Eu_3}{L} \end{pmatrix}$$

where the state vector $x = \begin{bmatrix} v_{c_1} & v_{c_2} & i_L \end{bmatrix}^T$ corresponds to the capacitors' voltages and the load current. The vector $u = \begin{bmatrix} u_1 & u_2 & u_3 \end{bmatrix}^T \in \{0,1\}^3$ represents the cells' states.

Nonlinear affine model:

The previous model can be also rewritten as a nonlinear affine model:

$$\dot{x} = f(x) + g(x)u \tag{2.9}$$

with

$$f(x) = \begin{pmatrix} 0 \\ 0 \\ \frac{R}{L} i_L \end{pmatrix}, \quad g(x) = \begin{pmatrix} -\frac{i_L}{C_1} & \frac{i_L}{C_1} & 0 \\ 0 & -\frac{i_L}{C_2} & \frac{i_L}{C_2} \\ \frac{v_{c_1}}{L} & \frac{v_{c_2} - v_{c_1}}{L} & \frac{E - v_{c_2}}{L} \end{pmatrix}$$

2.2.2 Average model

Average models for power converters have traditionally been used to get continuous models which simplifies the controller design compared to the use of the instantaneous model, in which continuous states (currents and voltages) coexist with discontinuous variables (state of switches).

The fundamental idea is to replace system variables with their average values throughout a switching period that is too short in comparison to the system's time constants. As a result, the generated model is continuous, allowing for the design of continuous controllers. Let us denote:

$$\begin{aligned} X(t) &= \langle x(t) \rangle = \begin{bmatrix} V_{c_1} & V_{c_2} & I_L \end{bmatrix}^T \\ U(t) &= \langle u(t) \rangle = \begin{bmatrix} U_1 & U_2 & U_3 \end{bmatrix}^T \end{aligned} \tag{2.10}$$

where $\langle x(t)\rangle$ and $\langle u(t)\rangle$ are the average values of the state and the input over a switching period T_s, defined as below:

$$\begin{aligned}\langle x(t)\rangle &= \frac{1}{T_s}\int_{t-T}^{T} x(\tau)d\tau \\ \langle u(t)\rangle &= \frac{1}{T_s}\int_{t-T}^{T} u(\tau)d\tau\end{aligned} \tag{2.11}$$

Therefore, the average model of a multicellular converter is given by:

$$\dot{X} = A(U)X + B(U) \tag{2.12}$$

with

$$A(U) = \begin{pmatrix} 0 & 0 & \frac{U_2-U_1}{C_1} \\ 0 & 0 & \frac{U_3-U_2}{C_2} \\ \frac{U_1-U_2}{L} & \frac{U_2-U_3}{L} & \frac{-R}{L} \end{pmatrix}, \quad B(U) = \begin{pmatrix} 0 \\ 0 \\ \frac{EU_3}{L} \end{pmatrix}$$

Now, the control signals are continous U_1, U_2, $U_3 \in [0,1]$, and they represent the duty cycle of each cell. With the same manner, the above model can be also rewritten as a nonlinear affine model:

$$\dot{X} = f(X) + g(X)U \tag{2.13}$$

with

$$f(X) = \begin{pmatrix} 0 \\ 0 \\ -\frac{R}{L}I_L \end{pmatrix}, \quad g(X) = \begin{pmatrix} -\frac{I_L}{C_1} & \frac{I_L}{C_1} & 0 \\ 0 & -\frac{I_L}{C_2} & \frac{I_L}{C_2} \\ \frac{V_{c_1}}{L} & \frac{V_{c_2}-V_{c_1}}{L} & \frac{E-V_{c_2}}{L} \end{pmatrix}$$

This model makes it easier to design indirect controllers that generate the average value of each cell's signal (also known as a duty cycle) and calculate the true cell's state using a pulse width modulator (0 or 1).

Remark 2.1:

The DC/AC multicellular converter can be modelled with the same approach as we did with the DC/DC version. Here is the average model of a three cells DC/AC converter (Fig. 2.2):

$$\dot{X} = f(X) + g(X)U \tag{2.14}$$

with

$$f(X) = \begin{pmatrix} 0 \\ 0 \\ -\frac{R}{L}I_L - \frac{E}{2L} \end{pmatrix}, \quad g(X) = \begin{pmatrix} -\frac{I_L}{C_1} & \frac{I_L}{C_1} & 0 \\ 0 & -\frac{I_L}{C_2} & \frac{I_L}{C_2} \\ \frac{V_{c_1}}{L} & \frac{V_{c_2} - V_{c_1}}{L} & \frac{E - V_{c_2}}{L} \end{pmatrix}$$

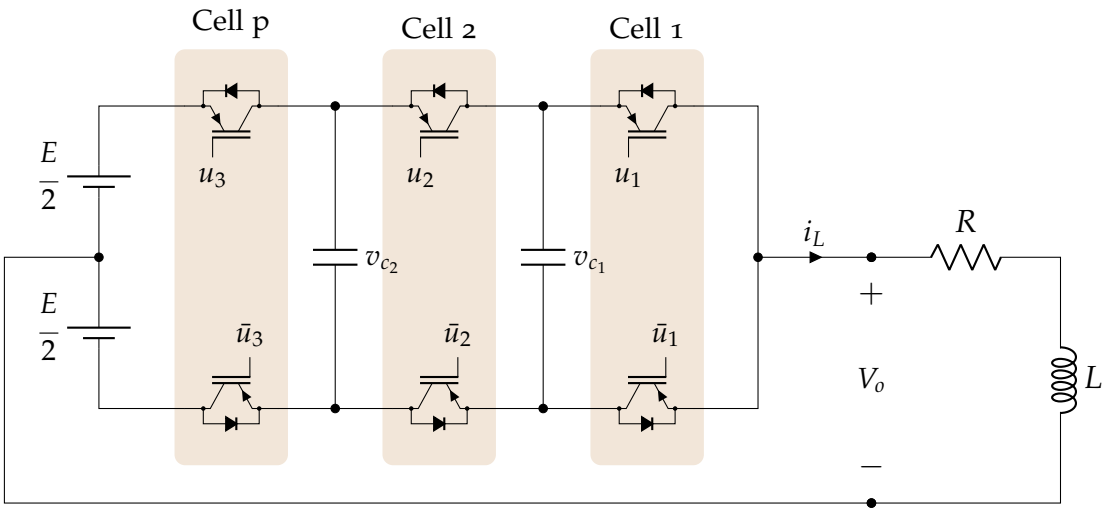


Figure 2.2: Multicellular converter associated with an inductive load.

2.3 Control design

In this section, we will design a nonlinear controller using input-output linearization. The idea of this approach is completely different from the conventional linearization based on Taylor series approximations. It is about solving the following problem:

Feedback linearization :

Consider a nonlinear system of the form:

$$\begin{aligned} \dot{X} &= f(X) + G(X)U \\ y &= h(X) \end{aligned} \tag{2.15}$$

Does exist a state feedback control law

$$U = \alpha(X) + \beta(X)v \tag{2.16}$$

and a change of variables:

$$z = T(X) \tag{2.17}$$

that transforms the nonlinear system into an equivalent linear system:

$$\dot{Z} = AZ + Bv \tag{2.18}$$

The principle is highlighted in Fig. 2.3 and in the next subsection, we will address this problem for the case of a multicellular converter and the reader may refer to [15, 16] for more details.

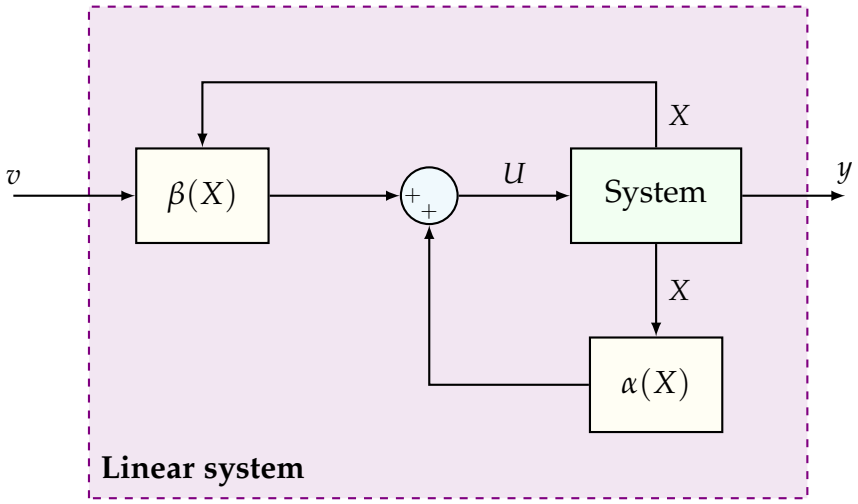


Figure 2.3: Representation of input–output linearization principle.

2.3.1 Feedback linearization design for 3 cells converter

From Eq. (2.13), the multicellular converter model is written as:

$$\begin{cases} \dot{X} = & f(X) + G(X)U \\ y = & h(X) \end{cases} \tag{2.19}$$

where the output of the converter corresponds to the whole state. Hence, we have:

$$y = h(x) = I_3 X \tag{2.20}$$

with I_3 is the identity matrix of dimension 3. The next step is to calculate the **relative degree** of each output. This can be calculated by differentiating the output of system r times to generate an explicit relationship between the output y and input u [16].

Relative degree:

Let us consider the first output:

$$\begin{aligned} y_1 &= V_{c_1} \\ \dot{y}_1 &= \tfrac{1}{C_1}(U_2 - U_1)\, I_L \end{aligned} \tag{2.21}$$

We remark that the input appears after one differentiation of the first output. Hence, the relative degree of this output is $r_1 = 1$.
Then, the second output:

$$\begin{aligned} y_2 &= V_{c_2} \\ \dot{y}_2 &= \tfrac{1}{C_2}(U_3 - U_2)\, I_L \end{aligned} \tag{2.22}$$

Thus, the relative degree of the second output is $r_2 = 1$.
Finally, for the third output, we have:

$$\begin{aligned} y_3 &= I_L \\ \dot{y}_3 &= \tfrac{1}{L}\left((U_1 - U_2)V_{c_1} + (U_2 - U_3)V_{c_2} + U_3 E - R I_L\right) \end{aligned} \tag{2.23}$$

The relative degree of the third output is $r_3 = 1$.

The total relative degree corresponds to the sum of the relative degree of each output:

$$r = r_1 + r_2 + r_3$$

From the fact that $r = 3$ which corresponds to the order of our system, we conclude that the model of the converter (2.19) is totally linearizable by feedback [16].

Linearizing feedback:

In this step, we are going to calculate the linearizing feedback:

$$U = \alpha(X) + \beta(X)v \tag{2.24}$$

where $v = [v_1\, v_2\, v_3]^T$ is the new input. From Eq. (2.21) - Eq. (2.23), we have:

$$\begin{aligned} \dot{y}_1 &= \tfrac{1}{C_1}(U_2 - U_1)\, I_L = v_1 \\ \dot{y}_2 &= \tfrac{1}{C_2}(U_3 - U_2)\, I_L = v_2 \\ \dot{y}_3 &= \tfrac{1}{L}\left((U_1 - U_2)V_{c_1} + (U_2 - U_3)V_{c_2} + U_3 E - R I_L\right) = v_3 \end{aligned} \tag{2.25}$$

To get the linearizing feedback (2.24), we need to solve the above system of equations with respect to U. The above system (2.25) is equivalent to:

$$\Delta(X)U(X) + \Delta_0(X) = v \tag{2.26}$$

with

$$\Delta(X) = \begin{pmatrix} -\frac{I_L}{C_1} & \frac{I_L}{C_1} & 0 \\ 0 & -\frac{I_L}{C_2} & \frac{I_L}{C_2} \\ \frac{V_{c_1}}{L} & \frac{V_{c_2} - V_{c_1}}{L} & \frac{E - V_{c_2}}{L} \end{pmatrix}, \quad \Delta_0(X) = \begin{pmatrix} 0 \\ 0 \\ -\frac{R}{L} I_L \end{pmatrix}$$

The solution of the system is given by:

$$U(X) = \Delta^{-1}(X)\left(v - \Delta_0(X)\right) \tag{2.27}$$

Hence, comparing this solution to Eq. (2.24) , we get:

$$\begin{cases} \alpha(X) = & -\Delta^{-1}(X)\Delta_0(X) \\ \beta(X) = & \Delta^{-1}(X) \end{cases} \tag{2.28}$$

Thus, the linearizing feedback is given by:

$$U = \alpha(X) + \beta(X)v \tag{2.29}$$

with

$$\alpha(X) = \begin{pmatrix} \frac{RI_L}{E} \\ \frac{RI_L}{E} \\ \frac{RI_L}{E} \end{pmatrix}, \beta(X) = \begin{pmatrix} C_1\frac{V_{c_1} - E}{EI_L} & C_2\frac{V_{c_2} - E}{EI_L} & \frac{L}{E} \\ \frac{C_1 V_{c_1}}{EI_L} & C_2\frac{V_{c_2} - E}{EI_L} & \frac{L}{E} \\ \frac{C_1 V_{c_1}}{EI_L} & \frac{C_2 V_{c_2}}{EI_L} & \frac{L}{E} \end{pmatrix} \tag{2.30}$$

Remark 2.2:

It should be noted that the inverse of the matrix $\Delta(X)$ exists if its determinant is not equal to zero. We have:

$$\det(\Delta(X)) = \frac{EI_L^2}{LC_1C_2}$$

This reveals two singularities, one when the input voltage is equal to zero and the other when the output current is null.

- The problem of the zero crossing of the input voltage will be solved simply

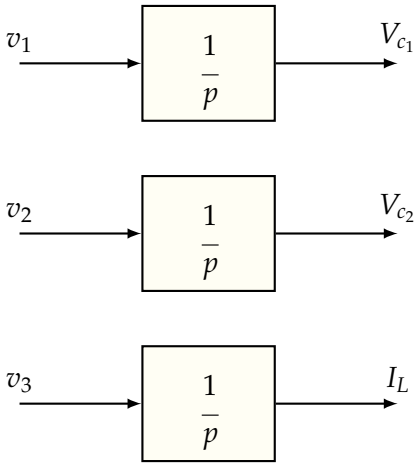


Figure 2.4: System after input–output linearization.

by supposing that, for such a system, we always work with an input voltage greater than 0.

- The problem of the current will be solved by blocking the linearization in the vicinity of zero current.

Outer loop design:

The converter under the control law Eq. (2.29)- Eq. (2.30) corresponds to a set of integrator (see Fig. 2.4):

$$\begin{aligned} \dot{y}_1 &= v_1 \\ \dot{y}_2 &= v_2 \\ \dot{y}_3 &= v_3 \end{aligned} \tag{2.31}$$

This means that we will use:

- v_1 to regulate the voltage V_{c_1} around $V_{ref1} = E/3$,
- v_2 to regulate the voltage V_{c_2} around $V_{ref2} = 2E/3$,
- v_3 to regulate the load current I_L around I_{ref}.

As we have constant references for the floating capacitor voltages and an integrator in open loop, a proportional action is sufficient, which achieves zero error in steady state. However, the reference load current is not necessary constant (sinusoidal in the case of DC/AC operation). To this end and to reject load variations (resistor variation), we will use a PI for the current loop (see Fig. 2.5).

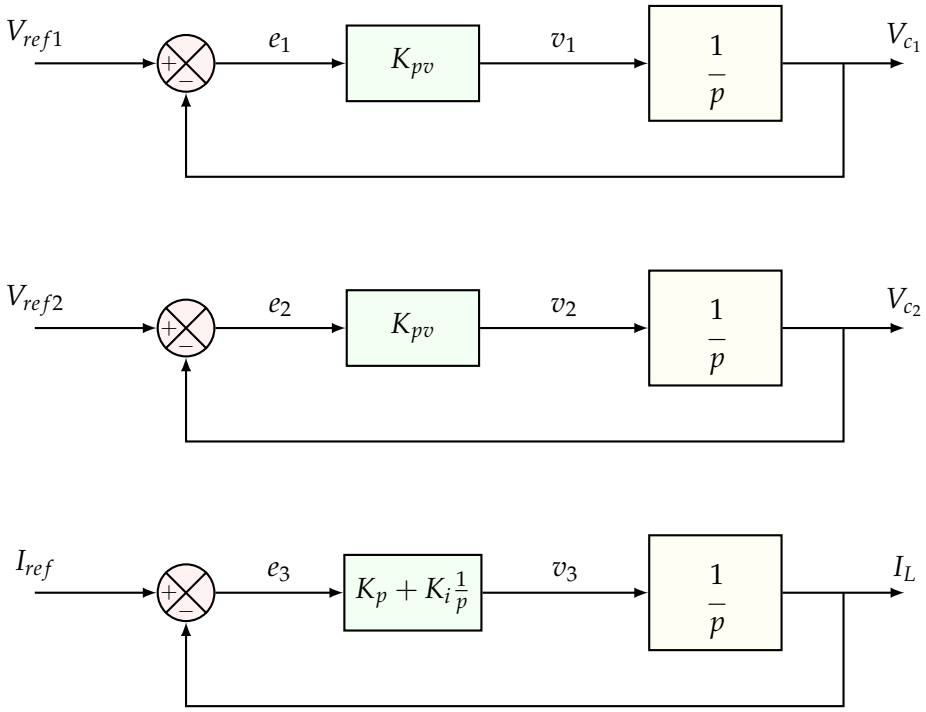


Figure 2.5: Outer loop control design.

Remark 2.3:

The choice of the proportional constant for the capacitor voltage loop is carried out by fixing a closed-loop dynamic for the system. The transfer function in closed loop is given by:

$$F_{CL}(p) = \frac{1}{\frac{1}{K_{pv}}p + 1} \tag{2.32}$$

The load current closed loop is given by:

$$F_{CL}(p) = \frac{K_p p + K_i}{p^2 + K_p p + K_i} \tag{2.33}$$

Compared to a second order system, we can get the controller parameters by fixing ξ and ω_0 as follows:

$$\begin{cases} K_p = & 2\xi\omega_0 \\ K_i = & \omega_0^2 \end{cases} \tag{2.34}$$

2.3.2 Feedback linearization design for 3 cells DC/AC converter

The three cells DC/AC converter model is given by:

$$\dot{X} = f(X) + g(X)U$$

with

$$f(X) = \begin{pmatrix} 0 \\ 0 \\ -\frac{R}{L}I_L - \frac{E}{2L} \end{pmatrix}, \quad g(X) = \begin{pmatrix} -\frac{I_L}{C_1} & \frac{I_L}{C_1} & 0 \\ 0 & -\frac{I_L}{C_2} & \frac{I_L}{C_2} \\ \frac{V_{c_1}}{L} & \frac{V_{c_2} - V_{c_1}}{L} & \frac{E - V_{c_2}}{L} \end{pmatrix}$$

which is similar to the model of DC/DC three cells converter (Eq. (2.13)) except the term $-\frac{E}{2L}$ in $f(X)$.

Following the same steps as we did in the previous subsection, we get the following linearizing feedback of DC/AC three cells inverter:

$$U = \alpha(X) + \beta(X)v \tag{2.35}$$

with

$$\alpha(X) = \begin{pmatrix} \frac{RI_L}{E} + 0.5 \\ \frac{RI_L}{E} + 0.5 \\ \frac{RI_L}{E} + 0.5 \end{pmatrix}, \beta(X) = \begin{pmatrix} C_1\frac{V_{c_1} - E}{EI_L} & C_2\frac{V_{c_2} - E}{EI_L} & \frac{L}{E} \\ \frac{C_1V_{c_1}}{EI_L} & C_2\frac{V_{c_2} - E}{EI_L} & \frac{L}{E} \\ \frac{C_1V_{c_1}}{EI_L} & \frac{C_2V_{c_2}}{EI_L} & \frac{L}{E} \end{pmatrix} \tag{2.36}$$

The outer loop design is similar to the DC/DC converter design part.

2.4 Conclusion

In this chapter, we presented the mathematical model of a three cells power converter associated with an inductive mode. The two structures of the converter (DC/DC and DC/AC) are considered and the difference between instantaneous model and average model is highlighted.

To meet the control requirements described in Chapter 1, we proposed a non-linear controller based on feedback linearization approach. The controller is designed based on the average model of the converter for the DC/DC and DC/AC versions.

In the next chapter, we will present the experimental setup of three cells converter which will be followed by simulation and experimental results.

Chapter 3

Experimental Setup

Contents

3.1 Introduction

This chapter presents the experimental workbench used for the verification and correctness of the control technique developed in the previous chapter. The Power converter design, construction, control and all experimental tests are conducted in LACoSERE laboratory at Laghouat University.

Fig. 3.1 shows the main parts of the test bench. The description of each element will be presented in detail in the following subsections.

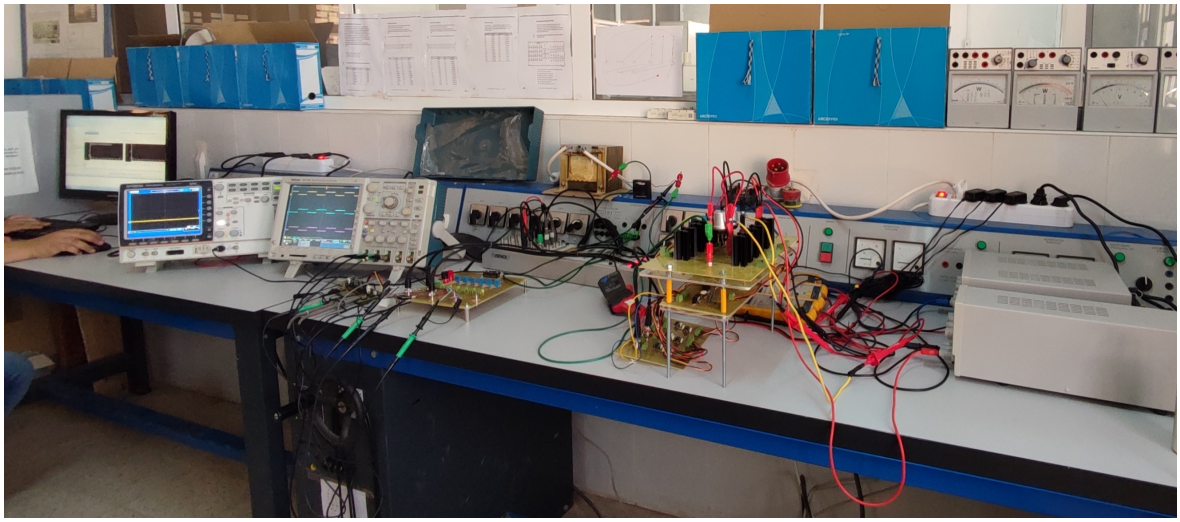


Figure 3.1: Experimental setup of 3-cells power converter.

3.2 Description of the Test Bench

In this section, we will present the test bench and the main hardware used in the validation process. As illustrated in Fig. 3.2, this test bench consists of:

- Multilevel three cells converter,
- dSPACE 1103 board,
- DSP 28335 Experimenter Board,
- PWM isolation and complementary signals generation board,
- DC-supply and PWM signals isolation,
- current and voltage sensors,
- Oscilloscopes,
- Isolated DC power supplies,
- Inductor and resistive load.

In the next sections, we will present each part with more details.

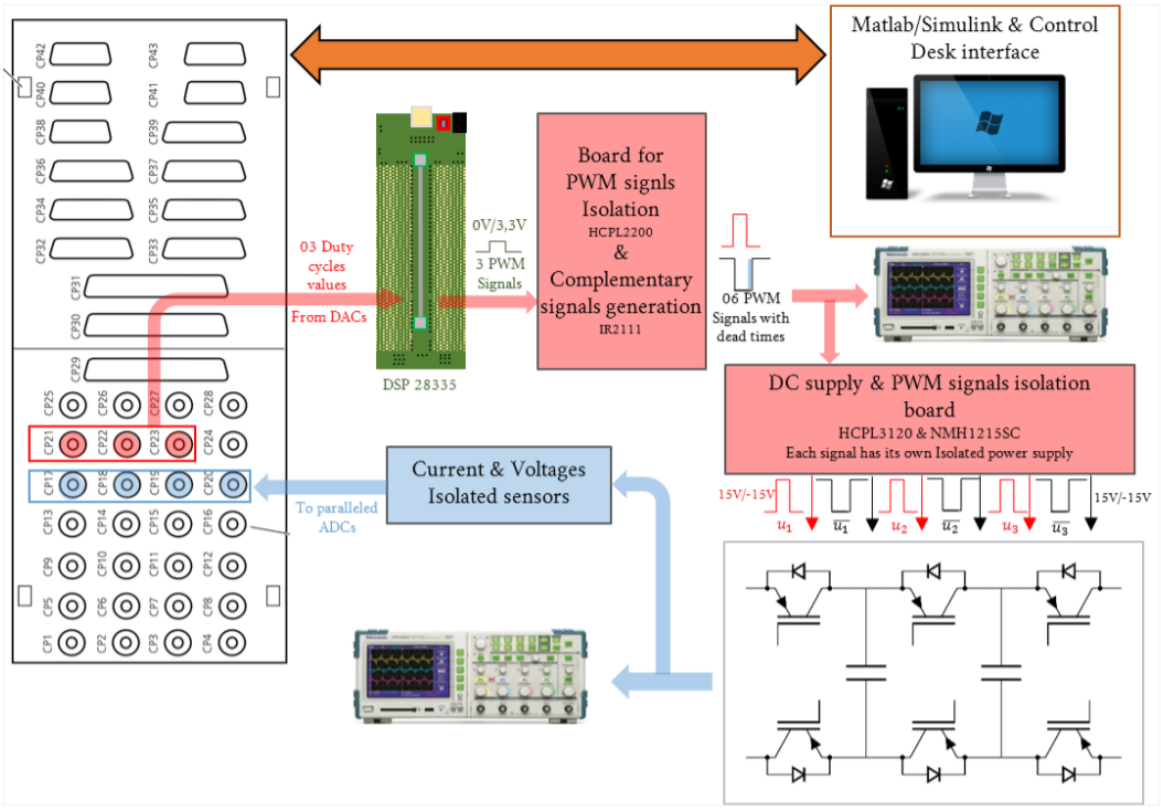


Figure 3.2: Schematic of the test bench.

3.3 dSPACE Board

The DS1103 is an all-rounder in rapid control prototyping. Its processing power and fast I/O are vital for applications that involve numerous actuators and sensors. Used with Real-Time Interface (RTI), the controller board is fully programmable from the Simulink® block diagram environment. You can configure all I/O graphically by dragging RTI blocks. This is a quick and easy way to implement your control functions on the board.

The controller board is designed to meet the requirements of modern rapid control prototyping and is highly suitable for applications such as induction motor control, robotics, positioning systems and stepper motors, active vibration control, and rapid control prototyping for automotive controllers. More specifications and information about the DS 1103 are summarized in Appendix A1.

In our experimental tests, the DS 1103 shown in Fig. 3.3 is used for:

- Measuring all the required signals, the output current of the multicellular power converter, the voltages of the floating capacitors and of the input source, which is achieved using parallel channels of the A/D converter.

Figure 3.3: dSPACE board.

- Displaying and storing, when needed, in real time the measured signals by means of the Control Desk software interface.
- Performing the control law by generating three duty cycles values, in real time, via the DACs connectors. The DACs (Digital to Analog Converters) can output voltages in the range of ±10volts. As the analog outputs are intended to be used as inputs in the DSP board, the output voltages are limited in Simulink, in order to generate voltages in the range of 0 to 3.3V[1].

[1]This is because ADCs of the DSP Board accept only voltages in the range from 0 to 3.3V.

3.4 TMDSDOCK28335 Experimenter kit board

It is a DIMM100 control card based on the DSP TMS320F28335 (see Fig. 3.4). A 32-bit MCU with 150 MIPS, 512 KB flash, and two 12b ADCs. It can generate 12 High Resolution PWM signals. The Board is used in this project **to generate three PWM control signals, shifted in phase by 120 degrees** from each other.

Remark 3.1:

This feature cannot be fulfilled by dSPACE board unless PWM signals are created and shifted in Simulink environment and then produced using DAC outputs. This solution is limited by Simulink sample time and leads to low-resolution and low-frequency PWM signals.

The three analog input signals, which come from dSPACE, determine the duty cycles of each generated PWM signal. The latter are used as inputs for the Isolation Board, which is also charged to generate the complementary PWM signals with dead-times.

Fig. 3.5 shows three PWM output signals of the DSP board shifted by 120 degrees from each other. These signals are obtained by sending a 0.5 duty cycle from the dSPACE, which corresponds to 1.65V.

Figure 3.4: DSP Board.

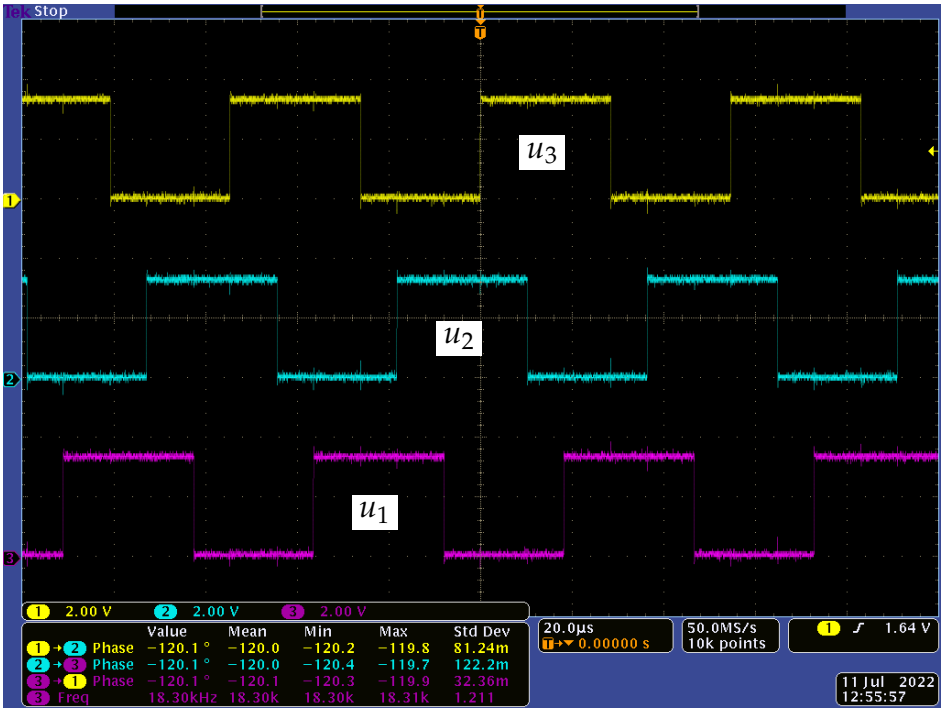


Figure 3.5: Three phase shifted output signals of the DSP-Board, 0-3.3V.

3.5 PWM-signal isolation & complementary signals generation Board

The board in question is shown in Fig. 3.6 which is used for safety reasons. Firstly, PWM signals are isolated and amplified by HCPL 2200 circuits in order to protect the controlling board (DSP Board) and to meet the inputs requirement of the IR2111 circuits, which produce complementary signals with dead-times of 700ns. This is a very important feature that protects the power converter from short circuits whatever the control signals are.

As the outputs of the IR2111 circuits are used as inputs for another Isolation board (and not to drive IGBT half bridge), the Bootstrap feature is disabled in order to make IR2111 produce both high and low sides signals as illustrated in Fig. 3.7:

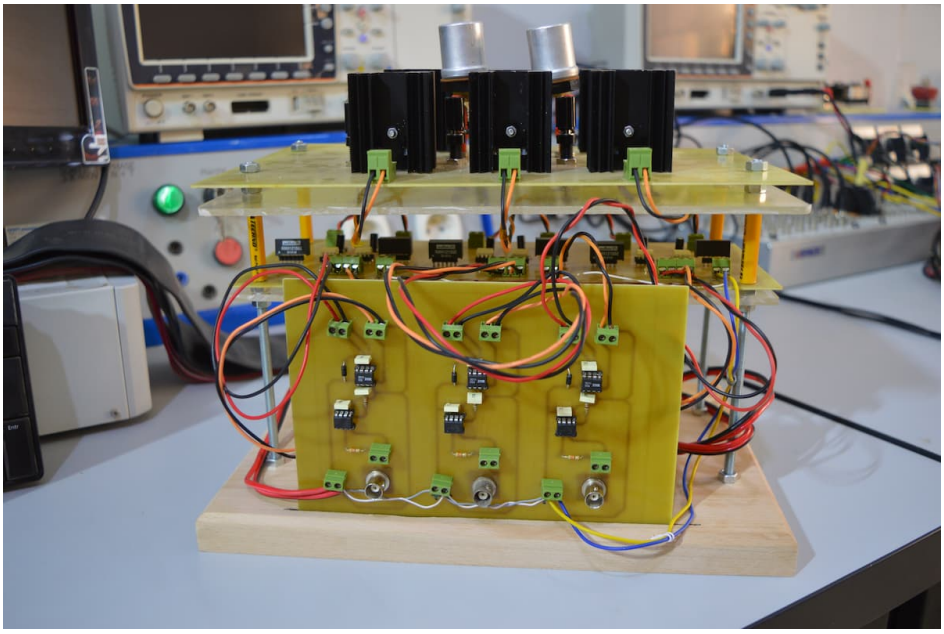


Figure 3.6: PWM Isolation and PWM Complementary generation Board

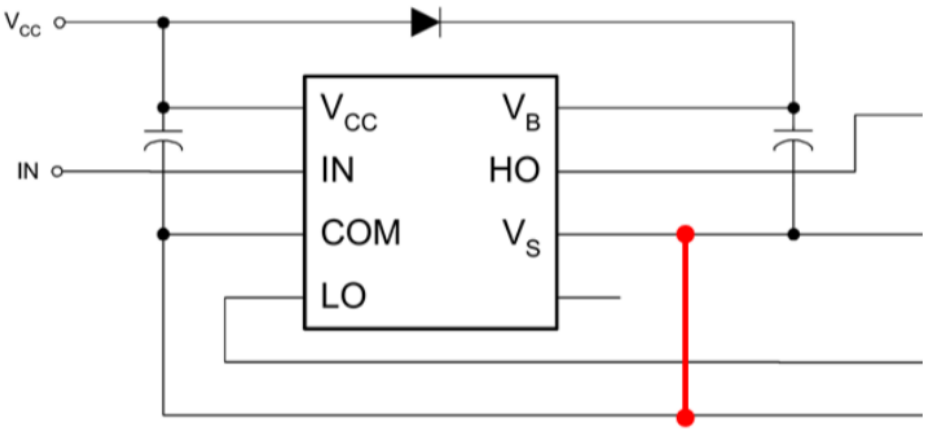


Figure 3.7: Disabling Bootstrap feature for IR2111 circuit.

Fig. 3.8 shows the Dead-time of two PWM complementary signals generated by the IR2111 circuit.

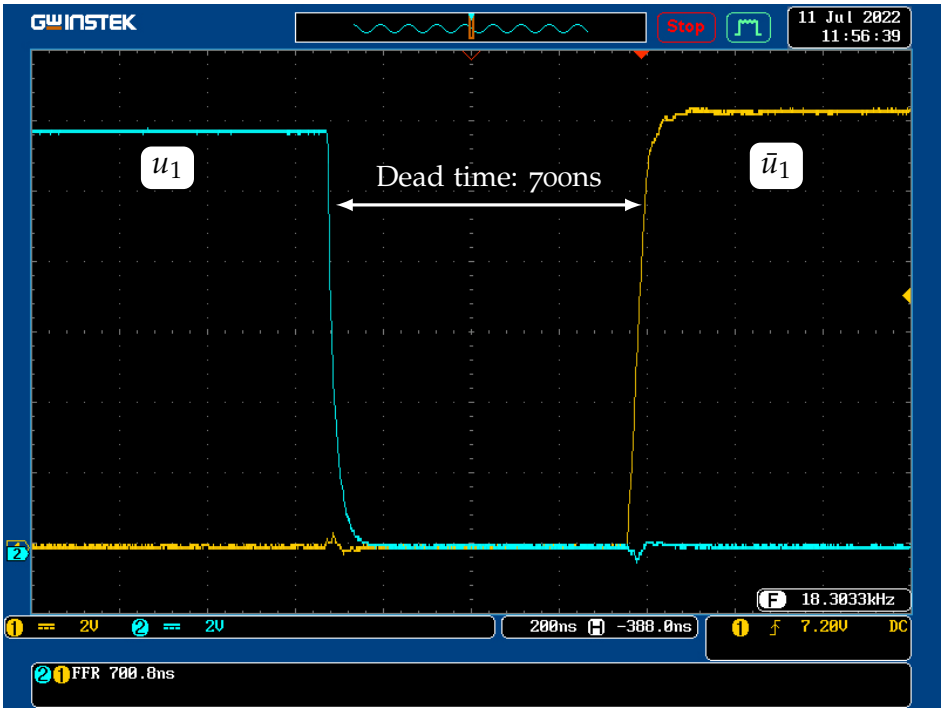


Figure 3.8: Dead-time of two PWM complementary signals produced by IR2111 circuit

3.6 DC supply & PWM-signals isolation Board

Thanks to the use of the NMH1215sc and HCPL3120 circuits, each PWM signal is produced with its isolated DC supply. PWM signals are generated with +15/-15 volt levels, which enhance the switch-off time of the IGBTs. Fig. 3.9 and Fig. 3.10 illustrate the developed board and an example of its output signal.

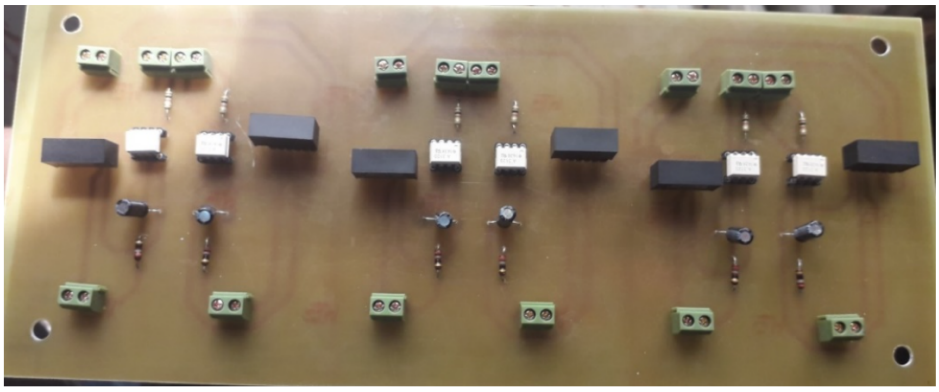


Figure 3.9: DC supply & PWM-signals isolation Board.

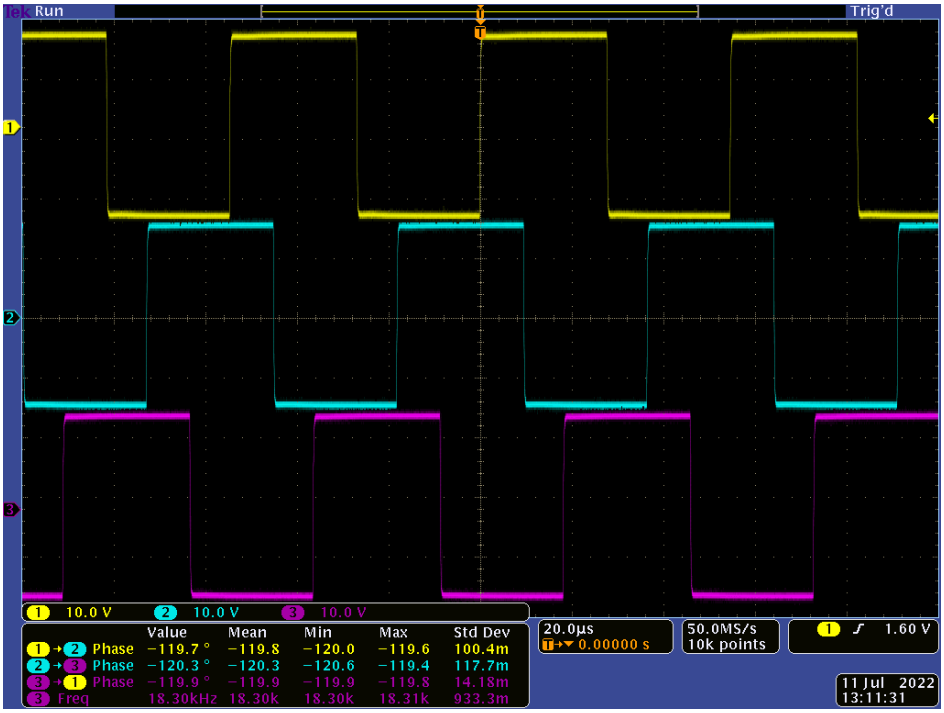


Figure 3.10: PWM shifted signals generated by the isolation Board (15V/-15V).

3.7 Multilevel three cells converter

Fig. 3.11 illustrates the experimental benchmark of a multicellular power converter:

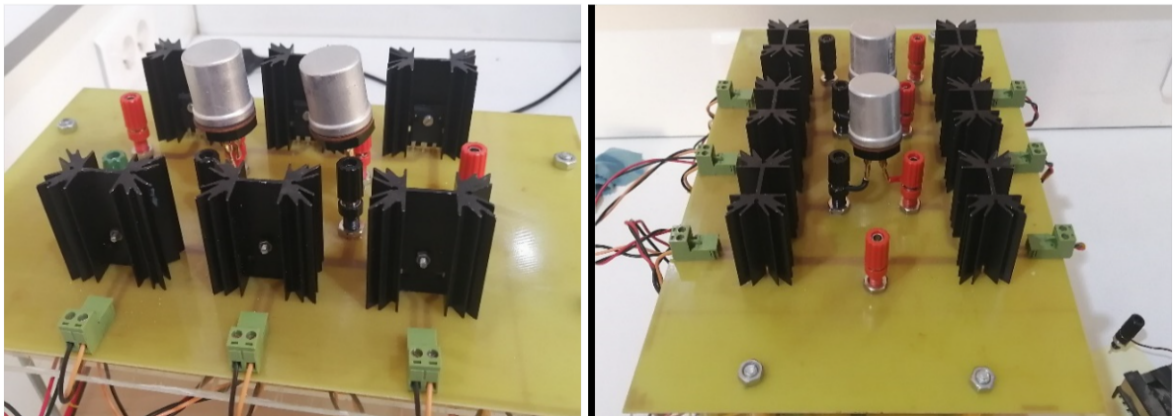


Figure 3.11: The developed Multilevel three cells Converter.

The developed Multilevel power converter is composed of three cells. Each cell is composed of two IGBTs (IRGP30B60KD). Between cells, there are two floating capacitors (100V, 50 µF) as illustrated in Fig 3.11.

The heat sinks, used to cool or dissipate the heat generated by IGBTs, are designed to handle low-electric power; therefore, the tests are performed under voltages less than 100

volts and currents less than 5 amps. Depending to the Load connection, the studied power converter can work as DC-DC Buck converter or as a single phase DC-AC converter.

3.8 Voltage and current Sensors

In order to ensure an isolation between the power stage and the control unit, we used for the measurements isolated voltage sensors that use optically isolated amplifiers designed specifically for voltage sensing, and Hall-effect based current sensors, which are galvanically-isolated sensors. Fig. 3.12 shows the sensors used in the experimental tests. At this level, we presented an overview about the developed experimental setup and the

Figure 3.12: Current and voltage measurement sensors.

next chapter will be devoted to testing the converter operation under the proposed control law.

3.9 Conclusion

In this chapter, we discussed different parts of the experimental setup which correspond to the converter and its auxiliary boards, the dSPACE and DSP control boards, and measurement devices. The control scheme developed in the second chapter will be implemented in the dSPACE board using Matlab/Simulink to test its effectiveness. This is the aim of the next chapter.

Chapter 4

Experimental Results

Contents

4.1 Introduction

In this chapter, we will test the experimental setup under the open loop control (See Chapter 1, operating principle). Then, we will check the effectiveness of the linearizing feedback on controlling the multicellular converter in two versions: DC/DC and DC/AC structure. It should be noted that the converter is a nonlinear MIMO system, MIMO stands for Multi Input Multi Output.

4.2 Experimental setup parameters

4.2.1 Power converter & load

The three cells converter is associated with an inductive load with the parameters: $R = 25\Omega$ and $L = 700\mu$H. These values are measured at the output of the converter using an LCR meter[1], shown in Fig. 4.1. This means that we took in consideration the inductor resistance as well as cables effect.

Figure 4.1: LCR meter.

The floating capacitors are chosen equal to 50μF and the input voltage E equals to 30V. The two control boards (Chapter 3, section 3.5 and 3.6) are supplied with 12V using a laboratory power supply.

4.2.2 dSPACE & DSP board parameters

The control law is implemented in Simulink/Matlab together with RTI blocks for measurement and duty cycle generation.

The sampling time is equal to 10μs and measured signals are processed with first-order lowpass filter with time constant $1ms$. This is justified by the fact the control law is designed based on the average model. Hence, it requires average values of the system states given by Eq. (2.11).

The dSPACE board sends average values of input signals (duty cycles) to the DSP. The latter generates 3 shifted PWM signals. The switching frequency is set to 18.3KHz.

[1] An LCR meter is a type of electronic test equipment used to measure the inductance (L), capacitance (C), and resistance (R) of an electronic component.

4.3 Open-loop control of 3 cells DC-DC converter

In the open loop control test, we will provide equal duty cycles for cells' control signals with $\frac{2\pi}{3}$ phase shift between them. Fig. 4.2 illustrates the implemented control law in Simulink/Matlab with RTI blocks.

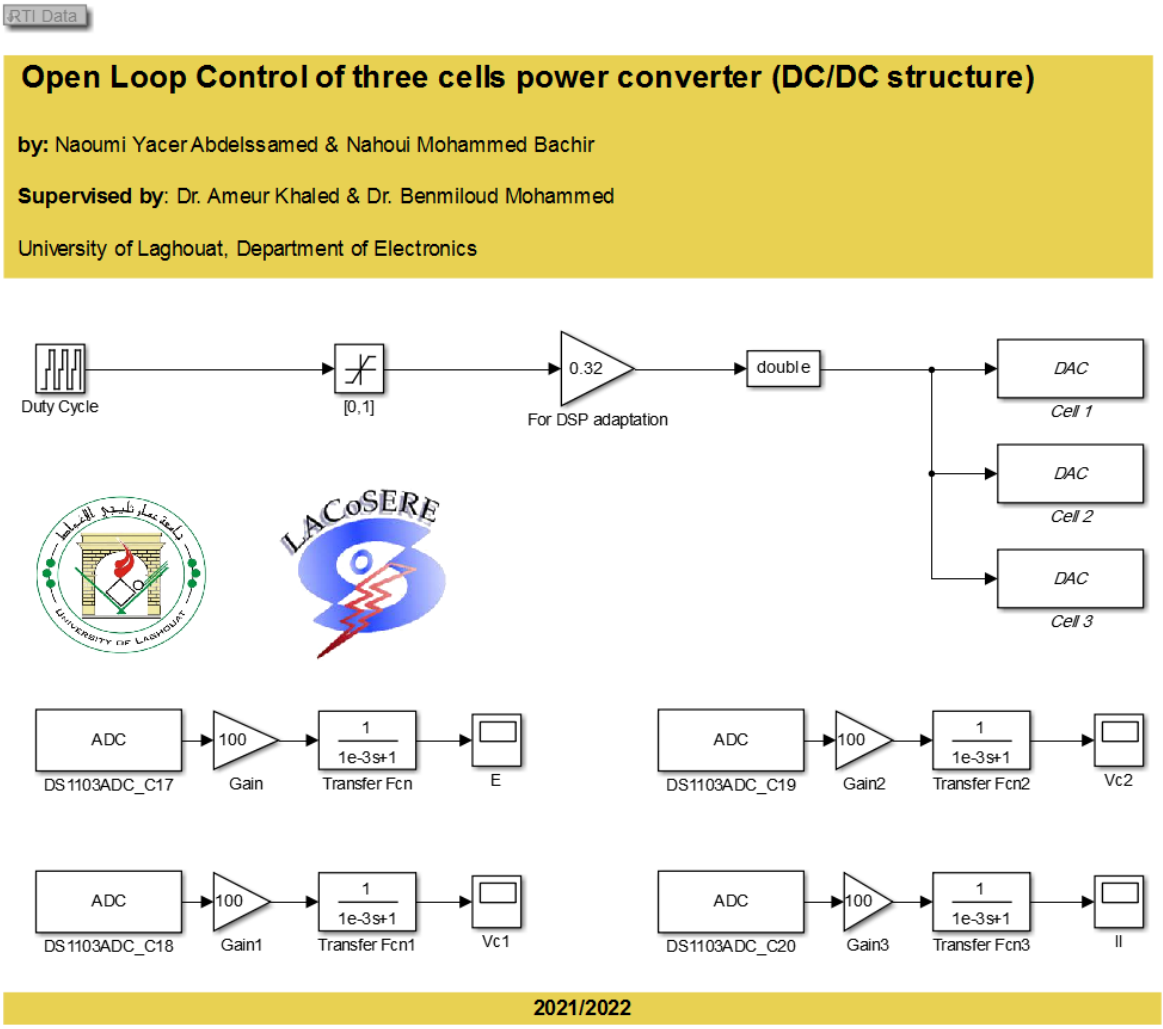


Figure 4.2: Open loop control implementation in Simulink/Matlab & RTI blocks.

The duty cycle is piecewise constant and it changes every 5s between the values: 0.2, 0.5 and 0.8. This corresponds to the following reference current values: 0.24A, 0.6A, and 0.96A. These values are obtained from the duty cycle expression [14]:

$$I_{ref} = d\frac{E}{R} \tag{4.1}$$

Fig. 4.3 illustrates the load current evolution which follows its reference with a remarkable error. It should be noted that this error decreases when duty cycle increases. The static

error returns to the fact that we considered ideal switches and capacitors in the modelling part.

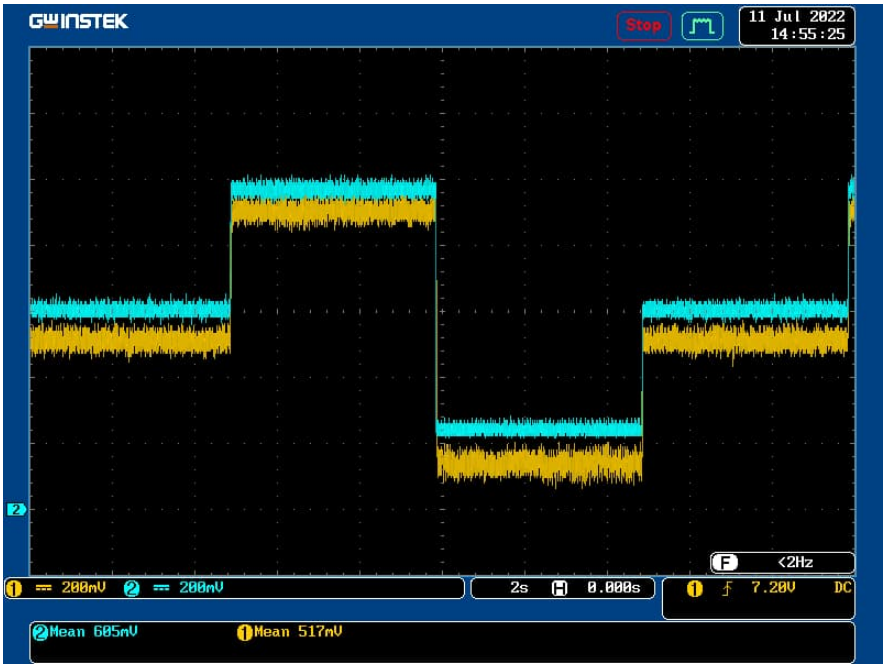


Figure 4.3: Load current in yellow and its reference in blue under open loop control.

Fig. 4.4 shows the measured voltages at the input and floating capacitors. One can notice the **natural balance** of the capacitor voltages due to the regular phase shift ($\frac{2\pi}{3}$) between input signals [2] .

4.4 Closed-loop control of 3 cells DC-DC converter

Fig. 4.5 illustrates the implemented linearizing feedback in Simulink/Matlab with RTI blocks. We will consider the same scenario as in the open loop control test (piecewise variations of reference current). Moreover, we will check the controller robustness under input voltage variations.

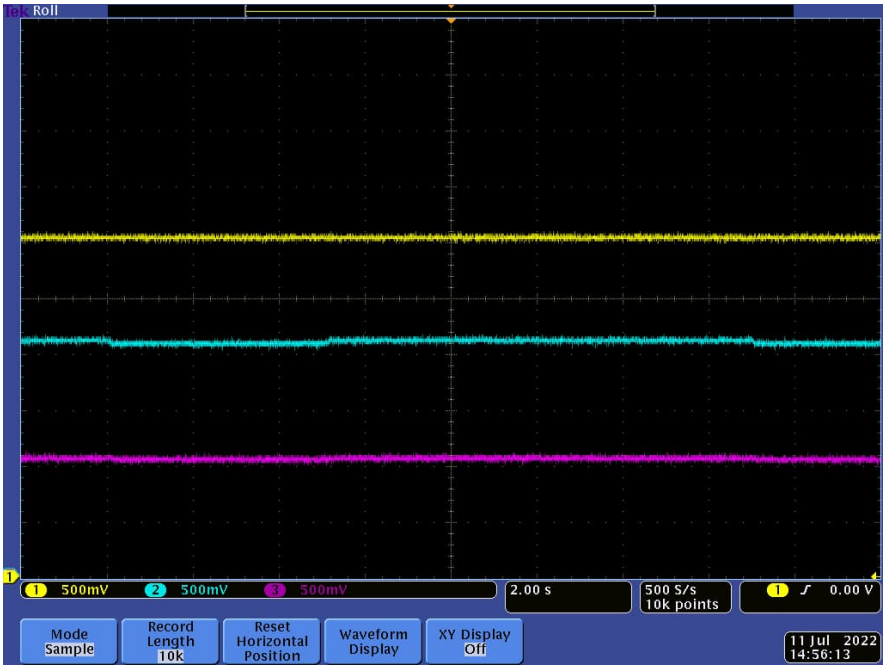


Figure 4.4: Input and floating capacitors measured voltages (open loop control).

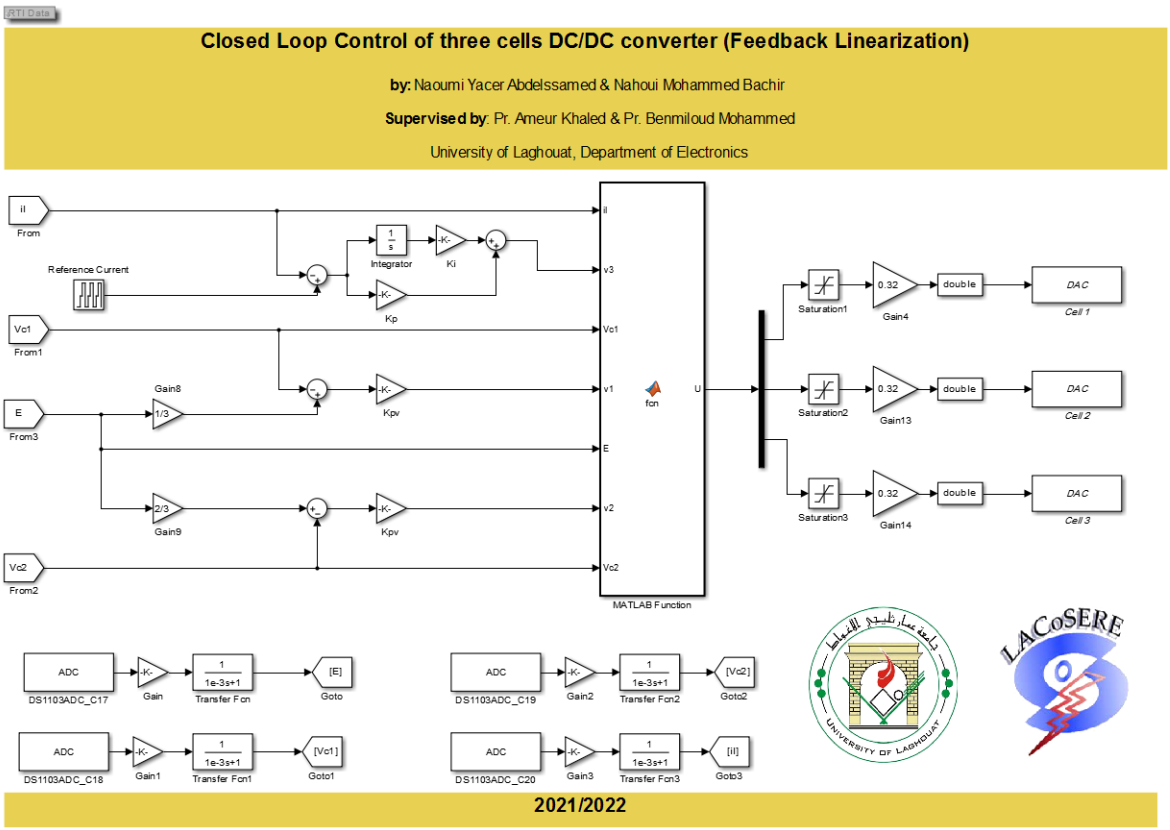


Figure 4.5: Closed loop control implementation in Simulink/Matlab & RTI blocks.

The controller parameters are chosen as follows:

- $K_{pv} = 5000$ which corresponds to 200μs time constant for the voltages' loops, Eq. (2.32), [12],
- $K_p = 1e5$, and $K_i = 1e4$ which corresponds to a damped response with response time 60μs. Fig. 4.6 illustrates the step response of the closed loop transfer function of the load current given by Eq. (2.33).

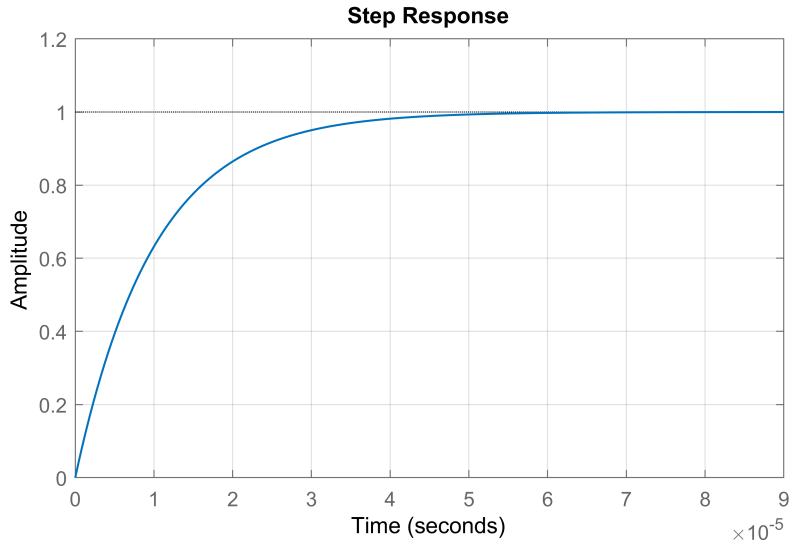


Figure 4.6: Step response of the closed loop transfer function of the load current.

4.4.1 Variable reference current

In this scenario, the DC input voltage is kept constant. The desired and measured load currents are presented in Fig. 4.7. We used the same reference current variations as in the open control loop test. We remark that the current response is very fast with zero error, in average, in steady state.

Fig. 4.8 presents the capacitors voltages and input voltage. One can remark that the controller achieves a good stabilization of the capacitors' voltages (V_{c_1} and V_{c2}) around their references (10V and 20V), respectively.

The output voltage of the converter is shown in Fig. 4.9. We can remark that Property 2 is verified. Indeed, in the first interval [0,5s] the reference current corresponds to a duty

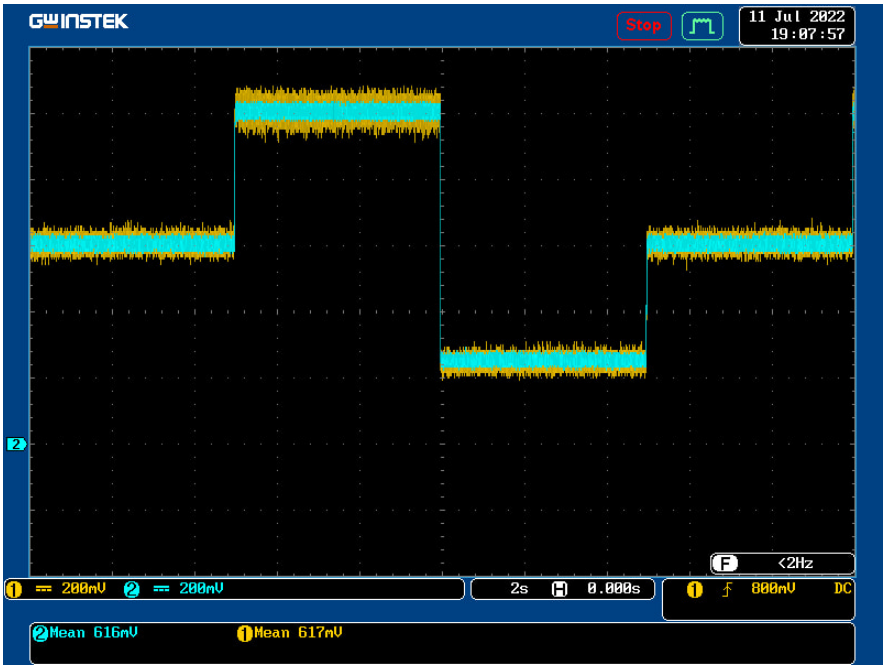


Figure 4.7: Load current in yellow and its reference in blue under closed loop control.

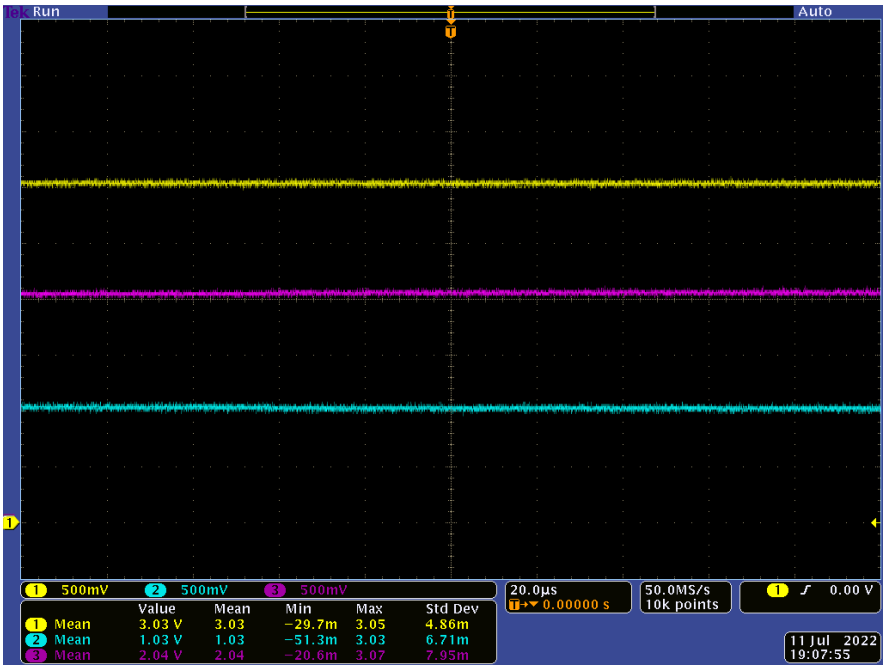


Figure 4.8: Input and floating capacitors measured voltages (closed loop control).

cycle of 0.5 which means that the output voltage oscillates between level 2 (10V) and level 3 (20V).

In the second interval [5s,10s] the reference current corresponds to a duty cycle of 0.8

which means that the output voltage oscillates between level 3 (20V) and level 4 (30V).

In the third interval [10s,5s] the reference current corresponds to a duty cycle of 0.2 which means that the output voltage should oscillate between level 1 (0V) and level 2 (10V). However, we remark some spikes to other levels which may be caused by the dead time.

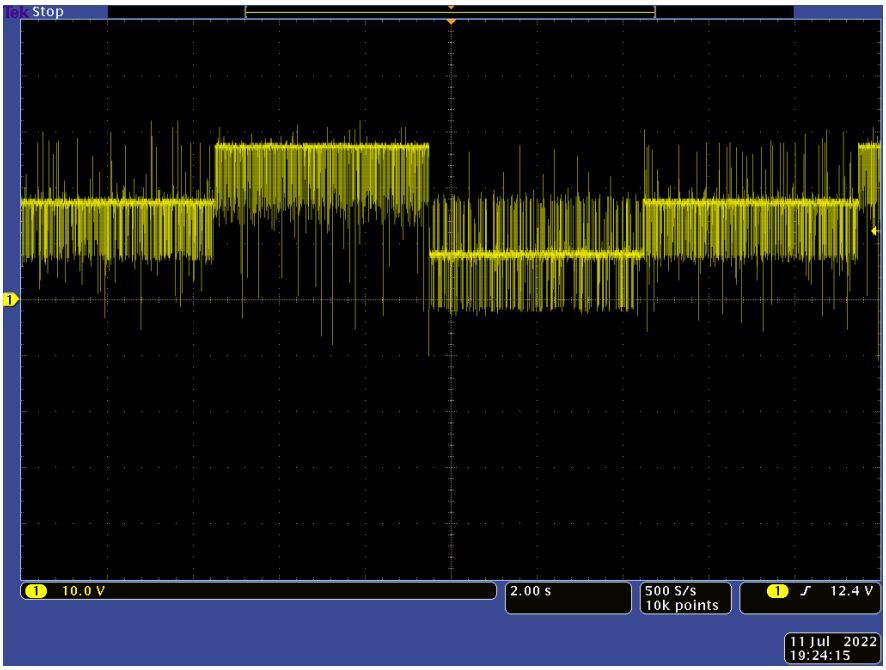


Figure 4.9: Output voltage of the converter.

4.4.2 Robustness against input voltage variations

In this test, we considered a variable input voltage with the same reference current as in previous tests.

The obtained results are shown in Fig. 4.10. It is clear that the controller is able to achieve a good stabilization of the load current despite the input voltage variations. Moreover, capacitors' voltages, V_{c_1} and V_{c_2}, follow their references, $E/3$ and $2E/3$, respectively. The input voltage variations were made manually using the laboratory DC power supply.

4.5 Closed-loop control of 3 cells DC-AC converter

The outer loop parameters of the capacitors' voltages have been changed from $K_{pv} = 5000$ to $K_{pv} = 100$. The outer loop parameters of the load current remain unchanged.

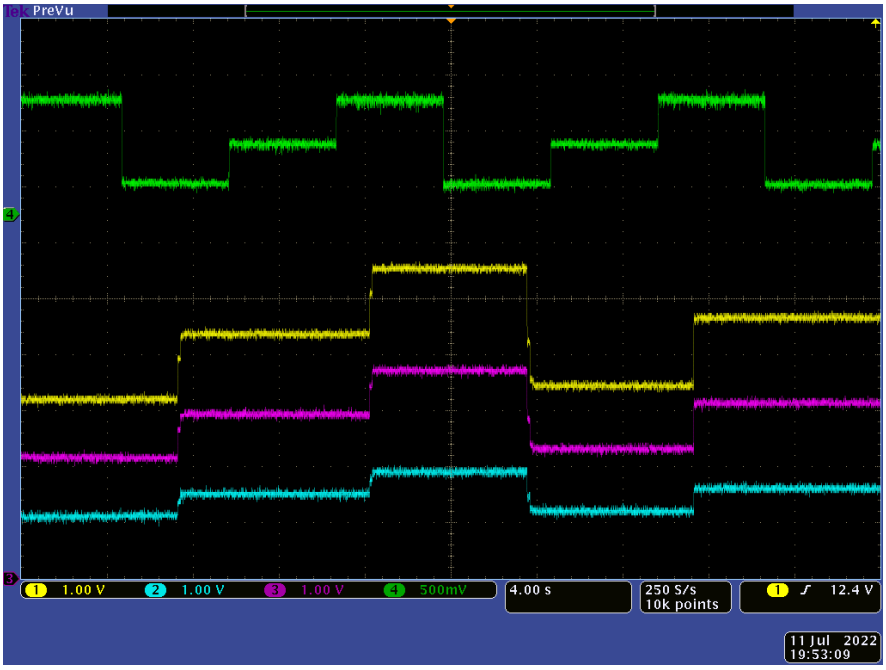


Figure 4.10: Obtained results under a variable input voltage.

Remark 4.1:

As we need a voltage midpoint at the input of the converter, we used a stabilized DC power supply with two outputs instead of two capacitors.
This returns to the fact that the capacitors' voltages at the input of the converter are not regulated and not considered in our control scheme. For that reason, in closed loop, one capacitor is discharged faster than the other one which affects considerably the output waveforms (voltage and current).

In this part and as a test, we have considered sinusoidal reference currents with 0.4A amplitude and two different frequencies: i) 1Hz frequency, and ii) 100Hz frequency.

Fig. 4.11 illustrates the load current and its reference. One can remark that the controller forces the output current to follow its reference, in average.

In Fig. 4.12, slight variations of 1Hz frequency are observed on capacitors voltages as well as input voltage due to the nature of the output current.

Fig. 4.13 and Fig. 4.14 illustrate a filtered version of the output current and voltages of the converter for a 100Hz reference current. One can conclude that the controller guarantees an acceptable system tracking of a given reference current and maintaining capacitors' voltages at their references.

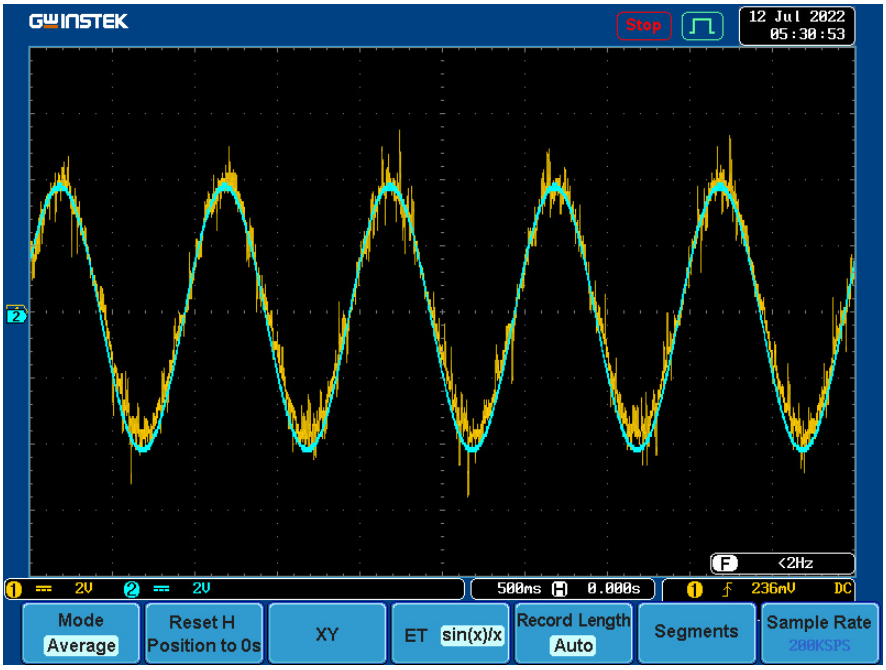


Figure 4.11: Load current and its reference of a DC/AC converter.

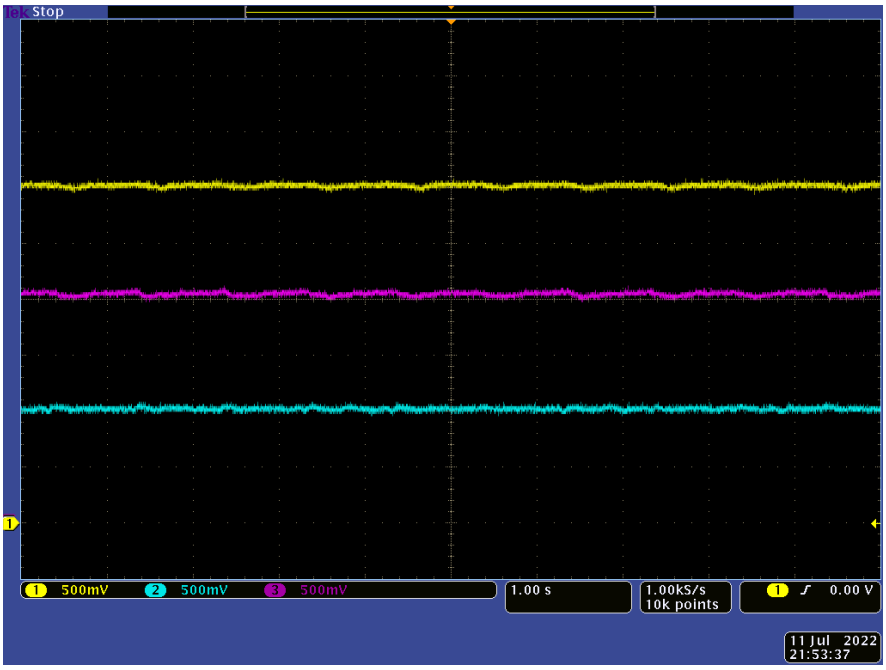


Figure 4.12: Input and capacitors' voltages of a controlled DC/AC converter.

In summary, the non-linear controller achieves good results in controlling the three cells power converter in its two versions: DC/DC and DC/AC. The capacitors' voltages are stabilized at their references and the output current is forced to track its reference.

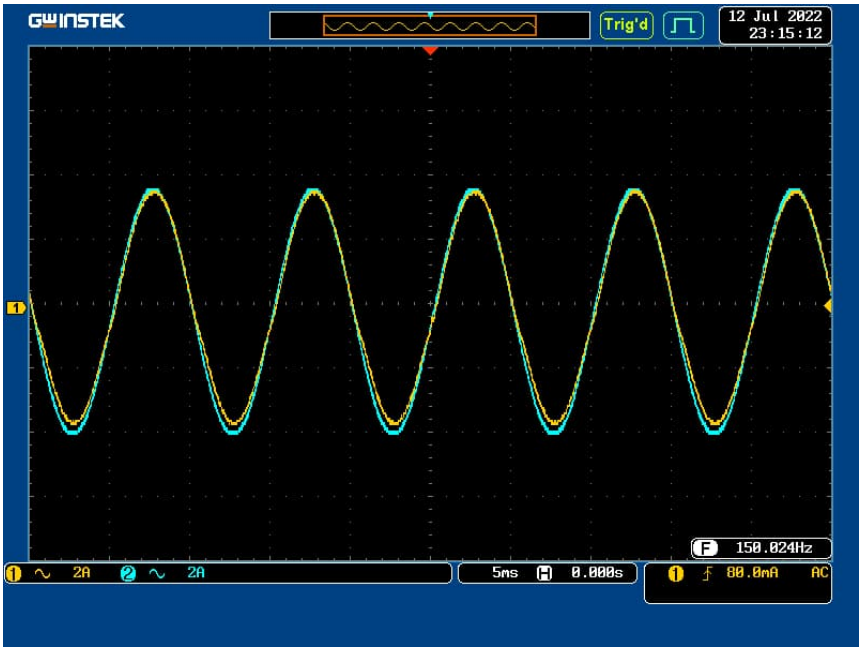


Figure 4.13: Load current tracking a 100Hz reference signal.

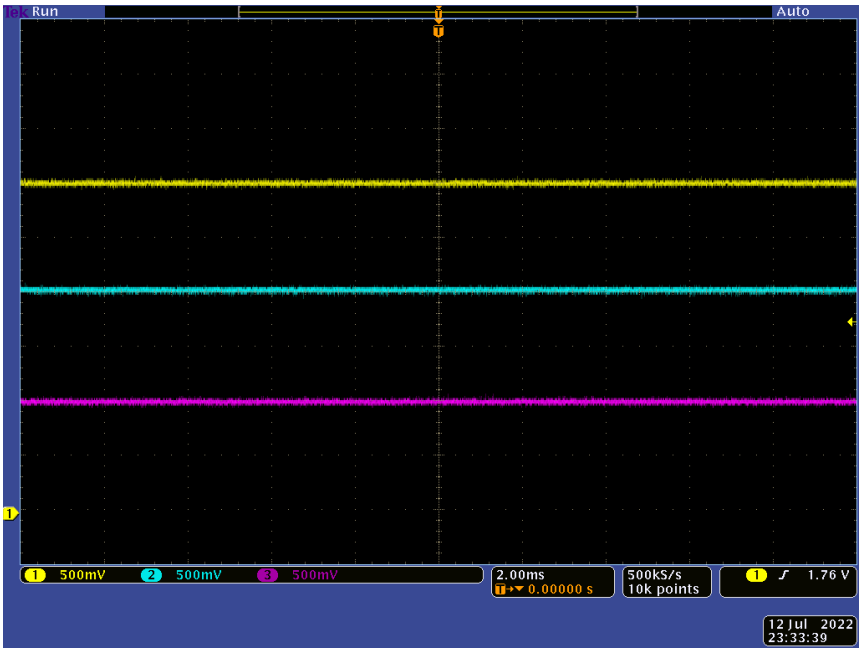


Figure 4.14: Input and capacitors' voltages of a DC/AC converter.

4.6 Conclusion

In this chapter, we have presented different experimental results. Firstly, the converter is tested in open loop to guarantee its correct operation and check the properties discussed in Chapter 1. Then, the nonlinear feedback linearizing controller is implemented in dSPACE

board and used to control the DC/DC three cells converter. Finally, we tested the nonlinear controller with the DC/AC version of the converter.

General Conclusion

This project is part of the work carried out within the Automatic Complex Systems Team of the LACoSERE laboratory on the subject of static converters control used for active filters. One of the objectives is to improve the electric energy quality using the power converter multicellular structure.

The work presented in this master thesis is devoted to the realization and control of three-cellular power converter in DC-to-DC and in DC-to-AC operation modes.

Firstly, chapter, we have introduced multicellular converters as well as their main properties. One of their many advantages is the reduction of the voltage across switches. This allows the use of faster switches which, in turn, guarantee high performance. The operating principle and control requirements of the multicellular structure was described.

Then, we presented the mathematical model of a three cells power converter associated with an inductive mode. The two structures of the converter (DC/DC and DC/AC) are considered and the difference between instantaneous model and average model is highlighted. To meet the control requirements described before, we proposed a nonlinear controller based on feedback linearization approach. The controller is designed based on the average model of the converter for the DC/DC and DC/AC versions.

After, we presented in details the different parts of the experimental setup which correspond to the converter and its auxiliary boards, the dSPACE and DSP control boards, and measurement devices. The control scheme developed in previous sections will be implemented in the dSPACE board using Matlab/Simulink to test its effectiveness.

and in the last section, we presented different experimental results. The converter is tested in open loop to guarantee its correct operation and check the properties discussed in Chapter 1. Then, the nonlinear feedback linearizing controller is implemented in dSPACE board and used to control the DC/DC three cells converter. Finally, we tested the nonlinear controller with the DC/AC version of the converter.

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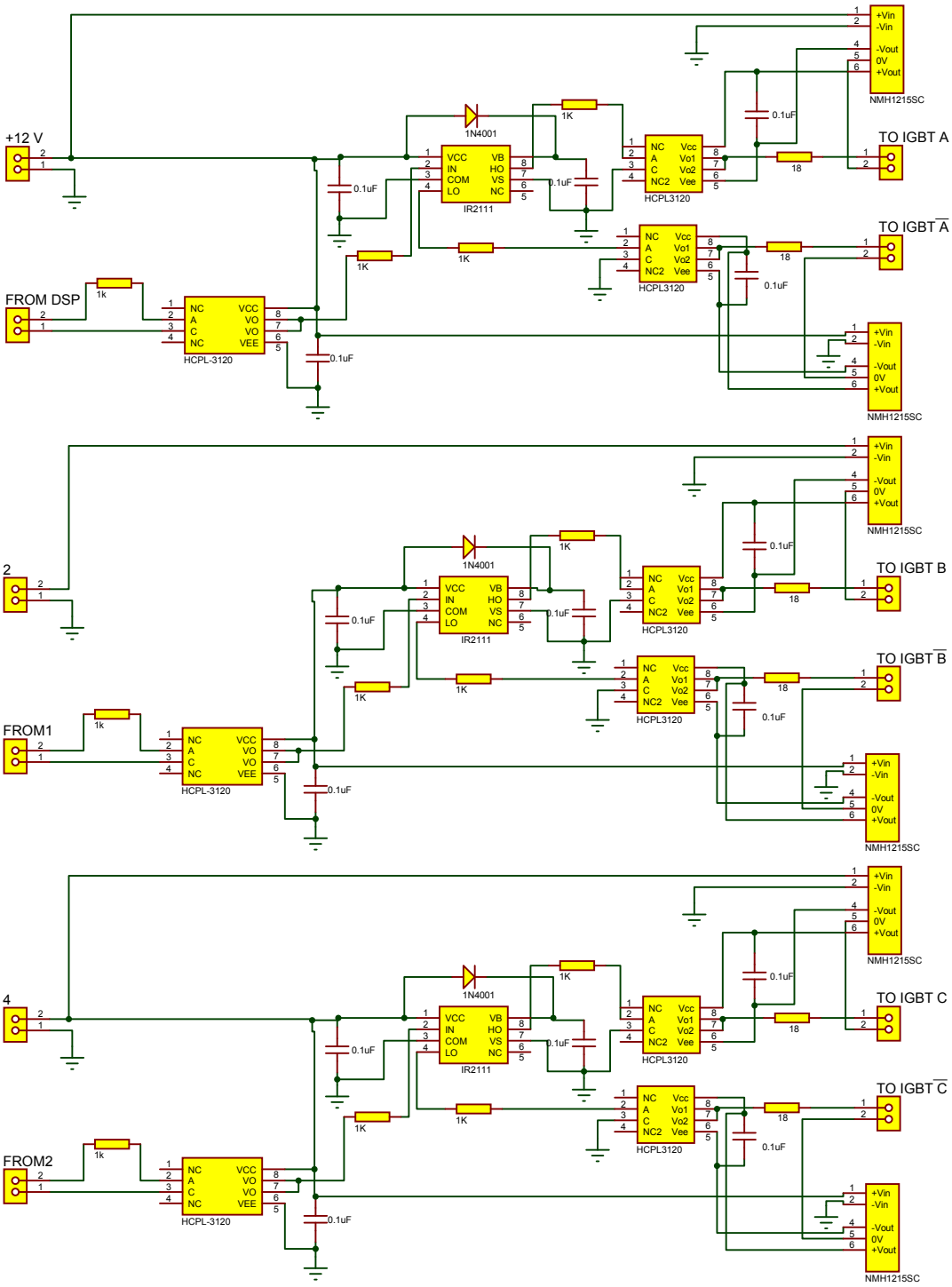
Appendix A

Datasheets

Isolation and amplification of PWM signals 0V/12V HCPL 3120 or HCPL2200

Generation of comlementary signals with dead times IR2111

DC supply Isolation for each PWM signal NMH1215 and HCPL3120



HEWLETT® PACKARD

2.0 Amp Output Current IGBT Gate Drive Optocoupler

Technical Data

HCPL-3120

Features

- **2.0 A Minimum Peak Output Current**
- **15 kV/μs Minimum Common Mode Rejection (CMR) at V_{CM} = 1500 V**
- **0.5 V Maximum Low Level Output Voltage (V_{OL}) Eliminates Need for Negative Gate Drive**
- **I_{CC} = 5 mA Maximum Supply Current**
- **Under Voltage Lock-Out Protection (UVLO) with Hysteresis**
- **Wide Operating V_{CC} Range:** 15 to 30 Volts
- **500 ns Maximum Switching Speeds**
- **Industrial Temperature Range:** -40°C to 100°C
- **Safety Approval**
  UL Recognized - 2500 V rms for 1 minute per UL1577
  CSA Approval
  VDE 0884 Approved with V_{IORM} = 630 V peak (Option 060 only)

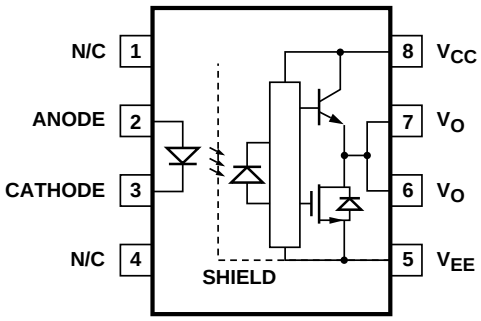
Applications

- **Isolated IGBT/MOSFET Gate Drive**
- **AC and Brushless DC Motor Drives**
- **Industrial Inverters**
- **Switch Mode Power Supplies (SMPS)**

Description

The HCPL-3120 consists of a GaAsP LED optically coupled to an integrated circuit with a power output stage. This optocoupler is ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The high operating voltage range of the output stage provides the drive voltages required by gate controlled devices. The voltage and current supplied by this optocoupler makes it ideally suited for directly driving IGBTs with ratings up to 1200 V/100 A. For IGBTs with higher ratings, the HCPL-3120 can be used to drive a discrete power stage which drives the IGBT gate.

Functional Diagram



TRUTH TABLE

LED	V_{CC} - V_{EE} "POSITIVE GOING" (i.e., TURN-ON)	V_{CC} - V_{EE} "NEGATIVE GOING" (i.e., TURN-OFF)	V_O
OFF	0 - 30 V	0 - 30 V	LOW
ON	0 - 11 V	0 - 9.5 V	LOW
ON	11 - 13.5 V	9.5 - 12 V	TRANSITION
ON	13.5 - 30 V	12 - 30 V	HIGH

A 0.1 μF bypass capacitor must be connected between pins 5 and 8.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

5965-4779E

International
IOR Rectifier

Data Sheet No. PD60028-M

IR2111(S) & (PbF)

HALF-BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- CMOS Schmitt-triggered inputs with pull-down
- Matched propagation delay for both channels
- Internally set deadtime
- High side output in phase with input
- Also available LEAD-FREE

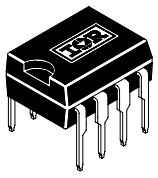
Product Summary

V_{OFFSET}	600V max.
I_O+/-	200 mA / 420 mA
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	750 & 150 ns
Deadtime (typ.)	650 ns

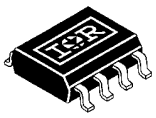
Description

The IR2111(S) is a high voltage, high speed power MOSFET and IGBT driver with dependent high and low side referenced output channels designed for half-bridge applications. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic input is compatible with standard CMOS outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Internal deadtime is provided to avoid shoot-through in the output half-bridge. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Packages

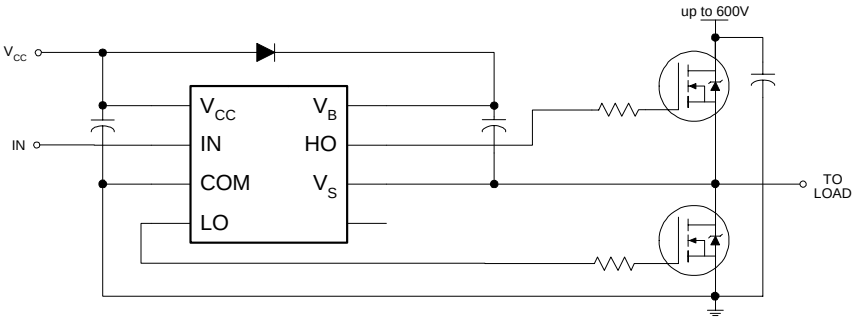


8-Lead PDIP



8-Lead SOIC

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

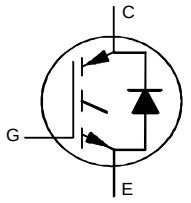
International
IOR Rectifier

IRGP30B60KD-EP

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Features

- Low $V_{CE\ (on)}$ Non Punch Through IGBT Technology.
- Low Diode V_F.
- 10µs Short Circuit Capability.
- Square RBSOA.
- Ultrasoft Diode Reverse Recovery Characteristics.
- Positive $V_{CE\ (on)}$ Temperature Coefficient.
- TO-247AD Package
- Lead-Free



n-channel

V_{CES} = 600V

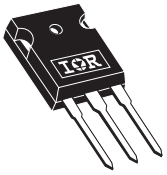
I_C = 30A, T_C=100°C

t_{sc} > 10µs, T_J=150°C

$V_{CE(on)}$ typ. = 1.95V

Benefits

- Benchmark Efficiency for Motor Control.
- Rugged Transient Performance.
- Low EMI.
- Excellent Current Sharing in Parallel Operation.



TO-247AD

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	60	A
I_C @ T_C = 100°C	Continuous Collector Current	30	
I_{CM}	Pulsed Collector Current	120	
I_{LM}	Clamped Inductive Load Current ①	120	
I_F @ T_C = 25°C	Diode Continuous Forward Current	60	
I_F @ T_C = 100°C	Diode Continuous Forward Current	30	
I_{FM}	Diode Maximum Forward Current	120	
V_{GE}	Gate-to-Emitter Voltage	±20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	304	W
P_D @ T_C = 100°C	Maximum Power Dissipation	122	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	—	0.41	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	—	—	1.32	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	—	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	—	40	
Wt	Weight	—	6.0	—	g